Kentech Instruments Ltd.

Electronics package for Hardened Gated X-Ray Detector [hGXD]

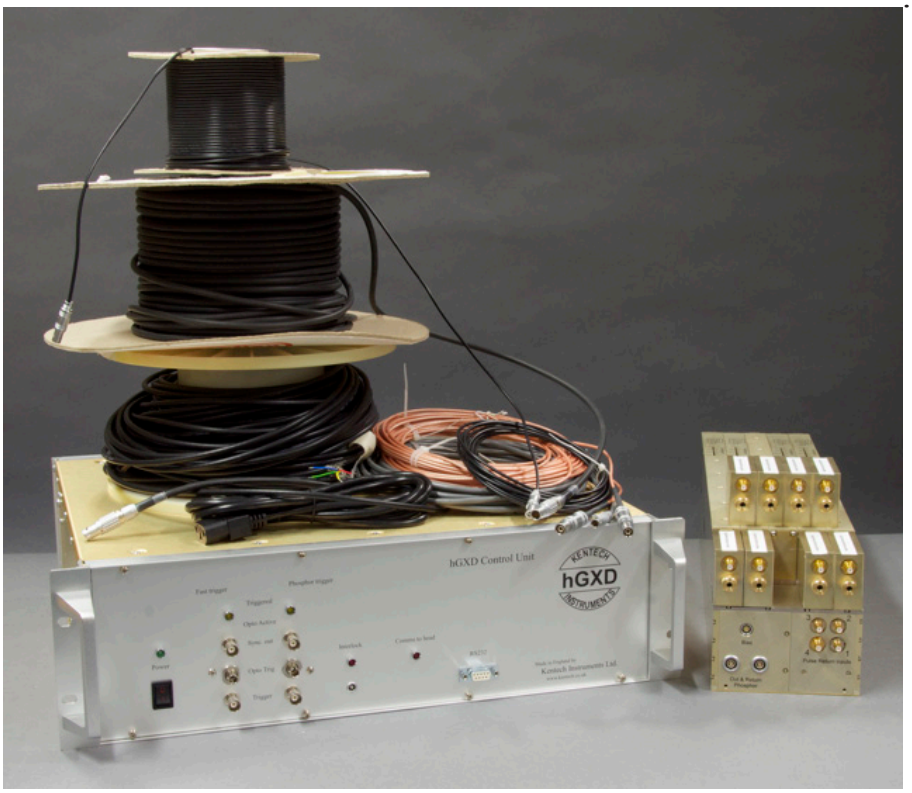
Serial Number J109123

Unit 3 (overall)

Last Modified 21-3-12

PLEASE READ THIS MANUAL CAREFULLY BEFORE USING THE PACKAGE

If familiar with hGXDs please read
Section 9.11 Changing the output voltage on page 20



Kentech Instruments Ltd.,
Isis Building, Howbery Park, Wallingford, Oxfordshire, OX10 8BA, U.K.
Tel: +44 (0) 1491 82 1601 Fax: +44 (0) 1491 82 1602
E-mail info@kentech.co.uk Web www.kentech.co.uk

Contents

Figure Captions

Tables

1 DISCLAIMER

This equipment contains high voltage power supplies. Although the current supply capacity is small, careless use could result in electric shock. It is assumed that this highly specialised equipment will only be used by qualified personnel.

Kentech Instruments Ltd. accept no responsibility for any electric shock or injury arising from use or misuse of this equipment. It is the responsibility of the user to exercise care and common sense with this highly versatile equipment.

2 VERSIONS

Version 17 was the first sent to the user.

Version 18 has updates regarding reading PFN identifying resistors.

Figure 1 Front and rear panels of the control unit

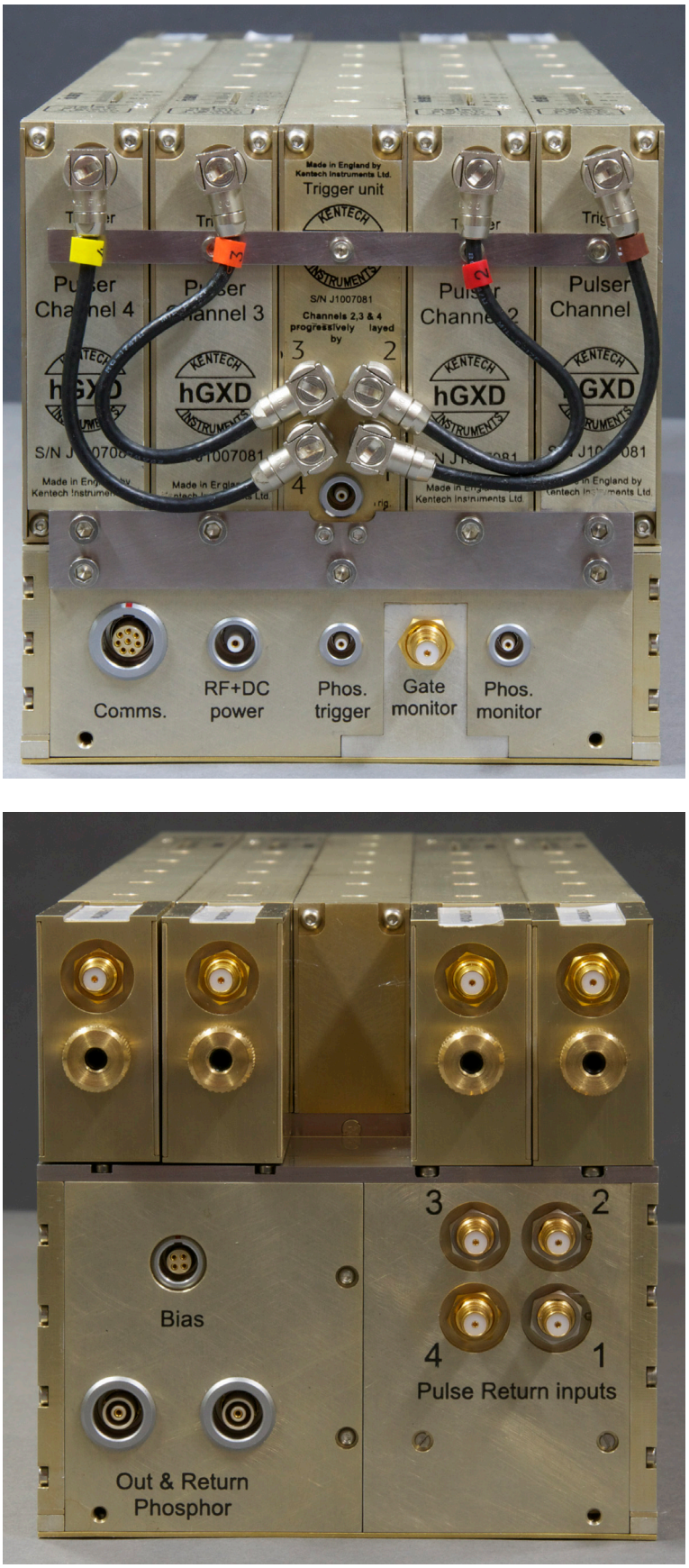


Figure 2 Front and rear panels of the head unit

Figure 3 Side view of head showing mount holes

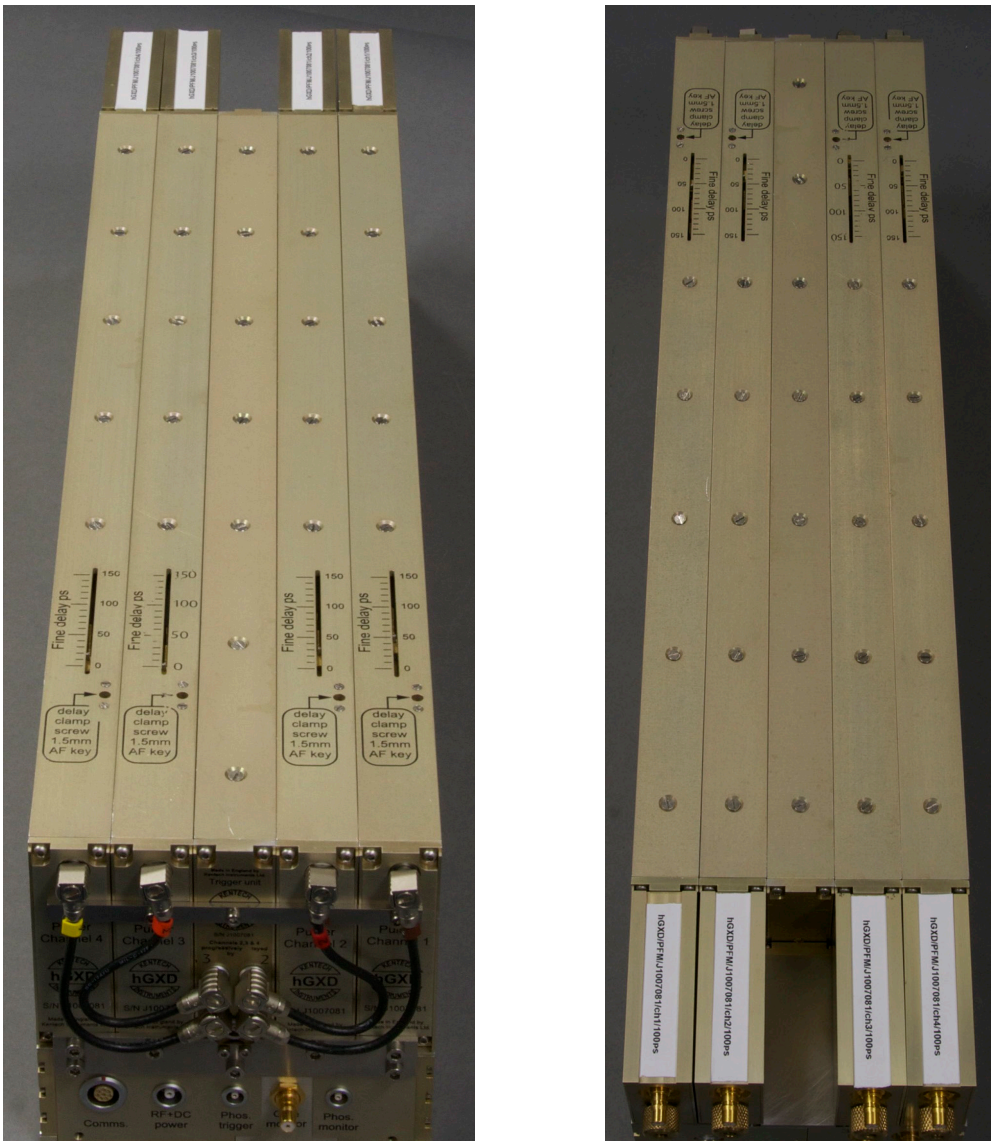


Figure 4 Top views of head

3 ABBREVIATIONS

ADC	Analogue to Digital Converter
dv	desired value
EEPROM	Electrically programmable and erasable Read only memory, non-volatile
EPLD	Electrically programmable logic device
EPROM	Electrically programmable read only memory, non-volatile
GXD	Gated X-ray detector, an earlier version.
hw	hardware
CU	Control module, 19 inch rack mounted unit
hGXDC	hGXD internal control system
mv	measured value
NIF	National Ignition Facility
PFL	Pulse Forming Line
PFM	Pulse Forming Modules
PFN	Pulse forming network, often the same as PFM
p-p	peak to peak
psu	Power Supply Unit or power supply.
RAM	Random access memory, volatile.
ro	read only
rw	read and write
SD	standard deviation
sw	software
UCS	Users Control System (to be provided by the user)
W/E	Write Enable
wo	write only

4 INTRODUCTION

This manual describes the operation and use of an electronics support package initially designed for the NIF Hardened Gated X-ray Camera. This package is expected to perform similarly to the GXD devices supplied already but is designed as a split unit with no delicate electronics near the camera head. This is to make the electronics more robust in the presence of a high neutron flux. This package is fully computer controlled via an RS232 link and with a suitable adapter via Ethernet. The package will deliver pulsed voltages to the load (the camera head). There are four channels. In addition the package will deliver bias voltages to each pulsed output on a single connector, and either DC or pulsed bias voltage for the phosphor.

5 DIFFERENCES BETWEEN hGXD and GXD

5.1 MECHANICAL DIFFERENCES

The hGXD being a split unit has both a head unit and a control unit. The control unit is in a standard 19 inch by 3U rack mount unit.

The hGXD head is very similar to the GXD head mechanically. The main outside dimensions of the boxes are the same, 114 x 114 x 491 mm^3. The mount holes down each side are in identical positions.

The types and positioning of the connectors is different. Drawings and a 3D model are included in this package. hGXD has 4 pulser modules and 1 trigger module whereas on GXD the trigger was combined into channel 1. The new arrangement allows us to have much greater trigger voltages and results in lower channel to channel jitter. With 5 modules (4 pulser and 1 trigger) the modules are slimmer than GXD pulser modules. Consequently the PFMs are slimmer on hGXD. hGXD PFMs should fit a GXD unit but not visa versa. The interface to the pulser is the same and the height is the same.

As hGXD has no Photoconductive detector provision there is one fewer connectors on the front face.

Note that the phosphor connectors are somewhat bigger to accommodate the higher pulsed voltage available.

5.2 ELECTRICAL DIFFERENCES

hGXD is a very different package electrically, the exception being the gate pulsers that are similar. Although the software interface has been designed to make the unit very similar to GXD the user and software developer should be aware of the differences which are caused mainly be the 21 second time it takes to write and read back from the head. Also as voltage regulation is by way of zener diodes instead of feedback amplifiers etc. the stability is such that repeated reads might be necessary. This cannot be fully automated as it is necessary to inhibit the trigger during a write-read cycle. As the system has no knowledge of when a trigger pulse might arrive it is important that it does not automatically disable anything.

1. The head unit has no embedded computer or sensitive logic. There is a separate control unit designed to be operated 50 metres from the head electronics.
2. In order to control up to ~ 78 variables and read back a similar number of parameters without a mass of wires, the head electronics incorporates an 78 bit relay based shift register. As a result it takes about 21 seconds to update the shift register with requested changes and then read back the values of the various variable. Boot up takes 41 seconds before the unit is ready to accept commands; this is because two write and read cycles are required before the unit is ready.

3 The unit is able to deliver a pulsed phosphor of up to ~ 10kV but the actual value will depend upon the total capacitance connected to the pulser. In particular the cabling from the package to the detector head and back will add significantly to the load capacitance. Using 75Ω cable will reduce this to about 56pFm^{-1}

4 In order to improve the system jitter and the channel to channel jitter and to limit the number of control lines, the pulser is arranged as a trigger module and 4 pulser modules. Each pulser module has its own delay unit. This is different from the GXD in which only 3 channels have delay adjustment.

This new arrangement delivers a much higher trigger voltage to the pulsers giving improved jitter performance. Observed cross channel jitter values are ~ 1ps standard deviation and ~7.5ps peak to peak.

The total delay adjustment on each channel is 10ns compared to 50ns on GXD. To permit the investigation of longer lived events (up to 19ns) the timing of the channels is staggered so that successive channels are triggered ~ 3ns later. As shipped the fine delays are set so that the channels are synchronous with the coarse delays set to 9, 6, 3 and 0 ns delay on channels 1, 2, 3 & 4 respectively.

This arrangement allows all the channels to be set up to be synchronous, or to cover a ~19ns event but with the channels being used in a preferred sequence (1 first through 4 last).

5 There is no longer an electronically adjustable fine delay as on GXD. This was of dubious use on GXD as the fine delay amount depended upon the coarse delay setting. On hGXD manual fine delays are provided for initial setting up. They use trombone type delay lines and are calibrated simply by the speed of light in air.

6 Voltage adjustment of the bias voltages is considerably coarser than on GXD. hGXD uses 50 volt steps from approximately -950 to +950 volts. Stabilisation is by way of zener diodes in the head rather than a feedback network. The stabilisation is not as good as GXD and has some initial thermal drift as the zeners warm up.

7 The phosphor voltage is similarly restricted. The phosphor DC voltage is up to ~ 2.9kV with the return lead connected. In pulsed mode it is capable of 10kV into a small capacitor. If the load capacitor is significant the available charge is shared between the internal capacitance (~3.7nF) and the load. E.g. a 3.7 nF external load will only receive half the voltage, see Figure 9 on page 19. There is no phosphor current trip.

8 Power to the head unit is by way of a single cable but this delivers both DC (~24 volts) and RF power (~100 volts peak to peak at up to ~ 0.5A, see Figure 30 on page 34.)

9 The user interface for hGXD and GXD are intended to be very similar. However, the user should note that a request for a specific bias voltage, for example, will be rounded off. In addition the response is slower. A write and read back cycle takes up to 20 seconds. Although this is transparent to the user as the user only writes to local memory in the control unit, the user should be aware that the unit may not be in the desired state for a little time after the request is made. There are register bits that indicate the current state of the device, i.e. whether it has updated the head with the requested data and whether the read back data is current. One can force a read back to make sure figures are current. One can also force a write so that the update is immediate. Several commands are put in for completeness but actually do nothing, e.g. current trip. The total current consumption actually returns the RF current only. The serial number algorithm is not implemented, instead a simple unit count number is returned. Unit number to serial number conversion can be carried out using the data supplied in the manual, see section 9.26 on page 37.

6 DIFFERENCES BETWEEN hGXD AND EARLIER VERSIONS

hGXD 3 has the ability to change the output voltage between two level by changing a slide switch rather than dismantling the unit and unsoldering wires. The switch does not switch the connection directly as a 5kV switch is needed, but drives a relay. Although the relay is rated at 5kV it is not designed to switch significant current. Consequently the slide switch should not be moved while the pulsers are power up. The ability to change the voltage easily means that it can be done, for example, when the PFMs are changed. Consequently PFNs can be tailored to specific voltage settings. This is likely to be particularly useful for the shortest pulses which tend to have a lower amplitude.

hGXD runs version V34 of the software (at the time of shipping). This version is basically like V32 but has some coding errors removed. The ADC is in the control unit and the ground connection to the head has significant series resistances (being 50m long). Consequently the ground voltage at the head depends upon the currents flowing to it. This would result in different voltages of measured parameters depending upon what was switched on. By measuring the voltage of the ground at the head this can be compensated for. V32 had some coding errors associated with this. V34 should give better results. It should be possible to use V34 in hGXD1. hGXD2 had a connection fault that was overcome by using V33 of the software, a special build that overrides the errors produced by the fault.

7 SPECIFICATIONS OF THE PACKAGE

Number of channels	4
Output pulse voltage	nominally 3kV but can be reduced to nominally 2kV by way of a switch on each pulser, see section section 9.11 on page 20
Output pulse duration	nominally 0.1 through 1ns with appropriate pulse forming modules
Trigger delay	This is very long due to the 50m cable from the control unit to the head unit.
Output pulse trigger delay range	nominally 10 ns on channels 1, 2, 3 and 4.
Output pulse delay offset	ch1 0ns, ch2 ~3ns, ch3 ~6ns and ch4 ~9ns
Minimum delay increment	~25ps
Power requirements	100 to 240 volts AC @ ~ 40 watts.
Dimensions	Head package 491mm (~19.33 inches) plus connectors long by 114mm (~4.49 inches) square. Control unit is 3U high, 19 inch rack mount by 410 mm deep.
Vacuum compatibility	The head electronics package has **NOT** been designed for operation under vacuum conditions.
Bias voltage on each channel	-0.95kV to +0.95kV nominal
Phosphor Voltage	0 to +2.9kV DC or 10kV pulsed (but dependent upon load capacitance)
Phosphor current trip	This is not supported.
Pulser monitors	The monitor inputs are designed for 100 volt operation. Four input, one output with nominally 4ns delay between channels. The attenuation through the combiner is a factor of 0.12. Channels 1 through 4 are mixed with progressively more delay.
Phosphor monitor	The phosphor return signal is fed to a separate monitor delivering nominally 100 volts per kV. The pulsed and

	DC calibrations will be slightly different. For a true waveform of the phosphor a fast high voltage probe should be used.
Maximum repetition rate	>40Hz gate pulse, 1Hz phosphor pulser.
Electrical trigger requirements	5 volts into 50Ω rising in < 5ns for both the main gate and phosphor triggers.
Optical triggering	Both fast gate and phosphor.
Wavelength	820 to 900 nm
	Optical power (on) -15dBm (min), +3dBm (max)
Optical Power (off)	-30dBm (max)
Width (50% level)	100ns (min), 250ns (max)
Rise time	<2ns
Maximum duty	0.1%

7.1 CONNECTORS ON THE REAR OF THE CONTROL UNIT

Power	IEC
Fast Gate trigger to head	N type
Phosphor trigger to head	BNC
Communications to head	Lemo EGG.1B.308.CLL
RF power to Head	Lemo PSA.0S.250.CTL.C32
Power ON indicator	Lemo ERA.0S.CTL

7.2 CONNECTORS ON THE FRONT OF THE CONTROL UNIT

Interlock	Lemo ERA.00.250.CTL
RS232	9 pin D type
Fast gate trigger	BNC
Phosphor trigger	BNC
Opto trigger, fast gate	Fibre optic ST jack
Opto Phosphor trigger	Fibre optic ST jack
Fast Gate sync. output	BNC
Phosphor gate sync. output	BNC

7.2.1 CONNECTORS ON THE HEAD UNIT

Pulse output	QMA x 4
Pulse monitor input	QMA x 4
Fast monitor output	QMA
Trigger from control unit	Lemo 00.250
Phosphor trigger from control unit	Lemo 00.250
Phosphor monitor output	Lemo 00.250
Trigger distribution on head	Lemo 00 250
Phosphor output	Lemo PSS 1S 408 CLL E37
Phosphor return	Lemo PSS 1S 408 CLL E37
Bias Output	Lemo ERD [ECP].0S.304.CTL
RF power	Lemo PSA.0S.250.CTL.C32
Comms	Lemo EGG.1B.308.CLL

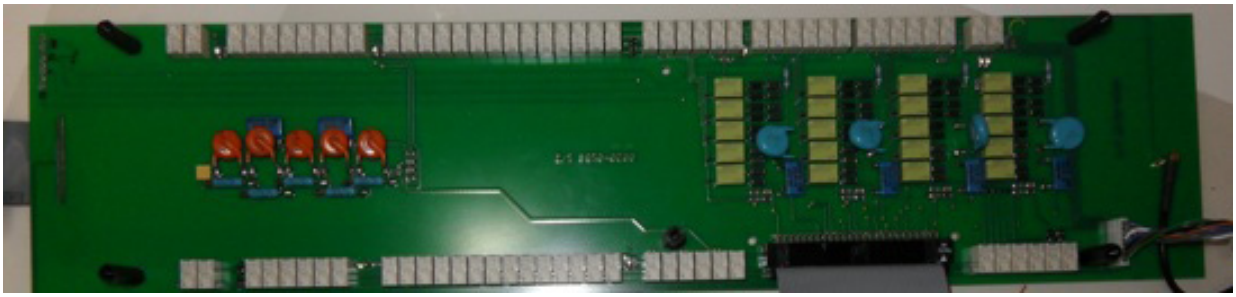


Figure 5 The shift register

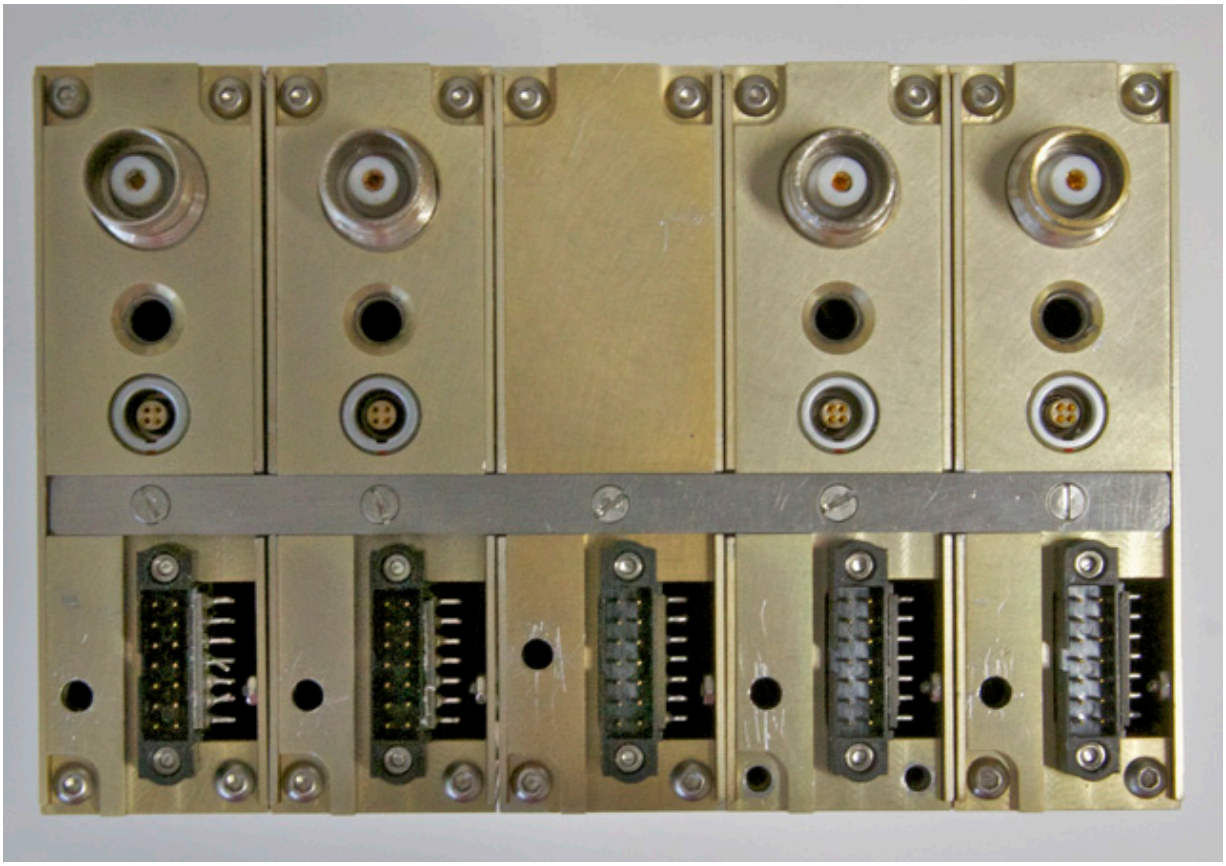


Figure 6 Pulser module to comms. module interface.
Note PFM ID connector key is downwards.

8 OVERALL DESCRIPTION

8.1 MECHANICS

The system comprises a head package and a control unit. These will be separated by ~ 50 metres of cabling. Suitable cable is provided except for the main trigger which needs to be run in high quality cable, e.g. LMR600. The power lead between the control unit and head module has a series resistance of 15Ω. If alternative cables are used the total resistance should be similar. i.e. neither significantly higher or lower. The head package consists of 6 modules, 4 pulse modules that are nominally the same, a trigger module and a comms. module which also incorporates the phosphor supply and the four bias supplies for the four channels. The modular structure allows the easy replacement of one pulser module and the ability to screen fully each channel and to ensure that cross talk is minimised. The pulse monitor return and combiner are attached to the bottom of the comms module as in GXD. The front and rear panels are shown in Figure 2 on page 6.

Whilst the four pulser channels are similar mechanically they have different identifying components to allow the control unit to select the correct delay calibration for the module. This is only checked at boot up time. The identifier components are hard wired internally and should not be changed without consulting the factory.

The assembly consists of the four pulser modules and trigger module strapped together and then fitted to the top of the rear section of the comms. module. The PFMs attach to the front of the pulser modules and rest on the top of the front section of the comms. module.

Mounting holes down each side of the comms. unit are provided, see Figure 1 “Front and rear panels of the control unit” on page 5.

The screws should not penetrate more than 5 mm into the sides.

The holes are not blind and the use of excessively long screws could easily result in damage or electrical problems.

The pulse length is set by the connection of a suitable Pulse Forming Module (PFM) to the output of a pulser module. The interface between the Pulsers and the PFMs is by way of modified TNC connectors. A normal jack is used on the pulser (with the thread machined back) and the PFM has a modified plug, it has had the clamp nut removed. The clamping action is achieved by way of a clamp screw on the PFM body. The PFM also connects to the Pulser module through a 4 way Lemo connector. This is solely for the purpose of PFM identification and will not affect operation of the system unless the UCS has been programmed to detect the PFM before proceeding.

8.2 ELECTRICAL CONNECTIONS

8.2.1 CONNECTING THE CAMERA HEAD

The following needs to be connected from the head electronics to the detector head:

1. Four gate pulse drives, one for each strip, from the PFMs, QMA
2. Bias lead carrying the four bias supplies, one for each strip, supplied, see Figure 7 on page 14.
3. Pulse return leads, QMA. The pulses should already be terminated, attenuated to the 100 volt level and stripped of their DC component.

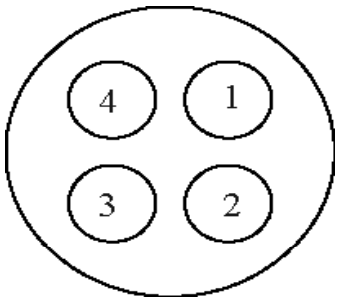


Figure 7 View into Bias output connector showing channel positions.

4 Phosphor out and return. These are identical as far as the head is concerned. The return enables continuity to be checked remotely. *Note that without the return lead the applied voltage will be higher than set.*

The bias voltages are capable of ±0.95kV. However, adjacent strips on the head will probably not tolerate such large voltages (up to 1.9kV between outputs). It is up to the user to make sure that the interstrip voltage is not too high. Note that this requires that the UCS knows the connection sequence of the channels to the head. It would be as well to always connect strips to corresponding channels so that no ambiguity can arise.

Do not connect or disconnect the head with a pulser running or the bias voltages on. Also do not run the pulser without connecting the pulser output to a load, generally through the head to the terminator, although for test purposes it can be connected directly to a suitable terminator.

8.2.2 CONNECTIONS BETWEEN THE HEAD ELECTRONICS AND CONTROL UNIT

There are four leads which connect the head unit to the control unit.

1 Power, Lemo FFA 0S.250 to same, this carries ~ 24 volts DC and ~ 50 volts RMS RF power. The lead has ~ 15Ω series resistance, this is intentional.

2 Communications, Lemo 1B.308 to same, this is a 8 way lead although only 7 ways are currently used. The spare is available for future modifications.

3 Gate Trigger, N type to Lemo 00.250 ~ 40 volts, on LMR 600, short lengths of thinner cable can be used at either end.

4 Phosphor Trigger, BNC to Lemo 00.250 ~ 24 volts RG58, LMR300 or similar.

8.2.3 CONNECTIONS BETWEEN THE HEAD ELECTRONICS AND THE OUTSIDE WORLD

There are 2 connections from the head to the outside word:

1 The pulse monitor, this is a combined set of all four pulses. (There is a factor of 0.12 attenuation in the monitor combiner).

2 Phosphor monitor, this delivers either the pulsed or a DC signal depending upon the setting of the phosphor. This signal is not buffered.

8.2.4 CONNECTIONS BETWEEN THE CONTROL UNIT AND THE OUTSIDE WORLD

There are 9 connections.

1 Power, IEC 100 to 240 volts AC at ~ 40 watts.

2 RS232 on 9 pin D type connector, see figure..

3 Interlock, short to enable of Lemo ERA.00.250.CTA

4 Main trigger, electrical, BNC, about 5 volts rising in ~ 1ns (5ns probably OK).

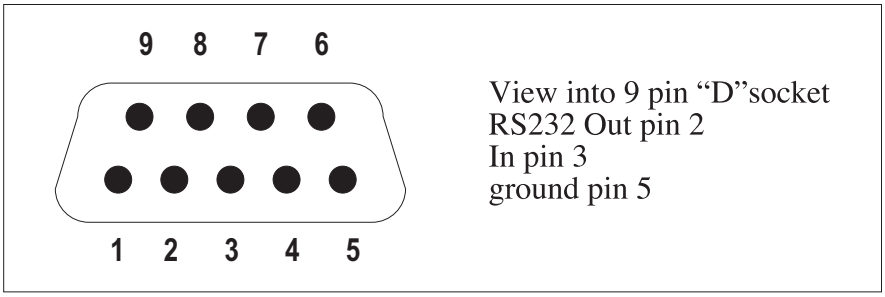


Figure 8 The pin out on the serial interface

5 Phosphor trigger, electrical, BNC, about 5 volts rising in ~ 1ns (5ns probably OK).

6 Main trigger optical, ST.

7 Phosphor trigger optical , ST.

8 Main trigger sync. output BNC

9 Phosphor trigger sync. output BNC

8.2.5 ELECTRICAL CONNECTIONS BETWEEN THE MODULES

The unit is supplied with the internal trigger leads in place on the rear panels of the pulsers. They are labelled for specific channels and are nominally the same. If they are swapped around small changes in the relative delays of channels. See Figure 2 on page 6 which shows the connections. Note that the timing of the trigger outputs to each module from the trigger module are different. They are staggered by ~3ns between successive outputs. It is important to connect them in a reproducible manner. Adhering to the diagrams and the labelling should help prevent timing mishaps.

8.2.6 EXTENDING THE EVENT COVERAGE TIME

If it is necessary to cover an event longer than 19ns, it is possible to use longer leads between the trigger module and the pulser modules. It is up to the user to sort out the cross timing calibrations in such a case. With small but high quality cable we would anticipate up to several tens of ns could be inserted. With a large format high quality cable some hundreds on ns ought to be feasible. No such tests have been made.

9 ELECTRONICS MODE OF OPERATION

9.1 PHILOSOPHY

The head electronics contains an 78 bit astable relay based shift register. Bipolar control lines are steered via this register to bistable relays that control various settings in the instrument. These control lines are also used to read back voltages from around the unit. Any relay in the shift register can control one bit of the instrument and read one bit. A single ADC back in the control unit is used to measure the voltages from the head unit and a second measures the voltage on the ground so that measurements are not affected by significant changes in ground return currents.

The power is supplied as RF at 100 volts peak to peak at up to 500mA and 24 volts DC is also available for measuring resistor values for unit identification and the delay confidence checking.

Although the implementation of the software is intended to make the complexities of the read and write cycles to the head transparent, it is important that the user understands that following a command to change something in the head unit there will be a delay before it happens. Also when trying to read the value of a parameter from the head the returned value will be the last one read back and this will not be current. One can force a write read cycle or wait up to 10 seconds for the tasker to execute a change. One can also force a read back cycle. Read back cycles are only executed following a write cycle or on demand. Write cycles disable the RF power and hence everything in the head. Read cycles disable the fast gate trigger and so should not be executed just before shot time.

A write cycle to the head is only executed following a change to a parameter in the head or on demand. For example if one sets a bias voltage to a voltage 100 volts then after about 20 seconds the bias voltage will be set to this value and the read back voltage will correspond to it. If however, the user waits a minute and then asks for the bias voltage again the same value will be returned because nothing has changed at the head and there have been no further read cycles. Of course in practice the actual value may have changed a bit due to thermal effects. So if a current value is needed it is necessary to force a read back from the head. Whilst a write to the head is followed by a read back,

the read back values may not be very stable as the RF power is removed during the write cycle and the zener diodes will have cooled a bit when the read back is made. For more accurate read back data the read back should be demanded a few minutes after a write cycle.

9.2 REGISTERS

As with GXD, the registers are the heart of the control system. There are four 16 bit registers as well as some internal ones. Some bits are read only some write only and some read and write. A write cycle copies the contents of all the registers to the head. A write cycle occurs ten seconds after a register value has changed that needs to be sent to the head. Within this ten seconds the user may change other register values and these will also be sent at the same time. If the user cannot wait ten seconds the write cycle can be forced.

9.3 BITS 3 AND 12 OF THE CONTROL REGISTER

The status of all the controllable parameters in the head is mirrored twice at the control unit (in silicon not relays). User commands are written to a local register (register 1). The system also keeps a copy of what is in the head in a mirror register (register 2). When the system detects a difference between registers 1 & 2 it starts a 10 second countdown, in addition bit 12 of the control register (not to be confused with registers 1 & 2) is set to zero. At the end of the countdown the contents of the local register 1, written to by the user, is copied to the head and to register 2. During this write cycle the RF is turned off so that no relay switches whilst current is flowing. After the write cycle the hGXDC checks to see if the local and head registers are now the same, if not it waits 10 seconds and starts again. If the local and head registers are the same, the RF is turned back on, the fast trigger is disabled and a read cycle is performed. At the end of the read cycle bit 12 of the control register is set to 1, indicating that the read back data is now valid. After requesting a read back bit 12 of the control register will indicate that the local read back value is invalid until the read back has finished at which time bit 12 of the control register will be set to 1 and the voltages can be read by the user with some confidence. The user only ever reads local values of the various parameters following a read back command. The only exception is the temperature which always gives a current value if bit 12 of the control register is set to 1, i.e read back is valid.

9.4 RF POWER

The turning on and off of the RF power is controlled by the software. Normally the RF power is on except during the write cycles. However, there is a “Disable RF on trigger” feature that allows the user to have the RF turn off following a shot. This is discussed at section 9.20 on page 35. If the RF has tripped on over current it can only be reset with a SAFE command which will also disable everything.

The amount of RF power delivered to the head depends upon what parts are enabled. This is to stop overheating in zener diodes when another section of the circuit is not running. For example less power is needed to run just the bias circuits than the bias circuits plus the pulsers. Without this control the zeners on the bias circuit would overheat. This is handled automatically by the system. If nothing is enabled the RF power is actually zero but the indicators show that it is running and active. The current measurement will show a very small value. This is why the **safe** command can be used to reset the RF power to ON, because although logically ON no power is sent as all the equipment is disabled by the **safe** command.

9.5 WRITE CYCLES

Write cycles will occur either on demand or 10 seconds after a register is changed that needs sending to the head unit. However, note that some bits in the control register are used locally in the control unit and consequently do not require a write cycle. These are the control of the electrical and optical

triggering of both the phosphor and the main trigger, enabling triggers (not high voltage enable, that has to be sent to the head), resetting trigger latches, setting RF disable on trigger. Consequently the user can set up a loop to reset the trigger latches after a trigger is detected without any delay for sending to the head.

If after a write cycle has finished the hGXDC decides that another write is needed it will be performed immediately, otherwise a read cycle is performed.

See e) “Control status bits:” on page 47 for which parameters require a write cycle.

During a Write cycle the RF power is disabled, all high voltages will be at zero and the head will not respond to triggers.

9.6 READ CYCLES

A read cycle is normally performed immediately after a write cycle. Read cycles are slower than write cycles because of some bandwidth limitations in the signal sent to the ADC. During a read cycle the RF power is enabled and its level will be set by the software to a relevant level for what is enabled, see 9.4 “RF POWER” on page 17. However, the fast trigger is disabled in the control unit during a read cycle. This is because we have found that the trigger delay is disturbed during the read cycle and decided that it is better the user knows that the pulsers will not work during the cycle.

The problem with this system is that the necessity to turn off the RF during the write cycle means that the zener diodes will be cooler during the read cycle than they are in normal use. This gives rise to poor values for the read back voltages etc. To overcome this one can force a read back at any time by setting bit 3 of the control register to 1.

9.7 INITIALISATION

On boot up the system checks to see what units are connected. It takes 2 write and read cycles because initially it is necessary to read with the RF power off. This is to find out which pulser modules are connected. Armed with this information the system looks up the delay calibration data for the pulsers fitted.

This is the only time the pulse modules are interrogated for IDs. If any IDs are changed the user should cycle the power on the control unit to force the system to record the module IDs. The pulser module IDs are used to correlate with delay data. Pulser module IDs should not be confused with Pulse Forming Module IDs.

During initialisation the hGXDC disables everything, sets all voltages to zero, sets the Phosphor to DC mode and the triggering to electrical mode on both inputs; delays are set to zero. The user should then set things as wished. This initialisation takes 41 seconds and during this period the unit is unresponsive.

9.8 RUNNING THE ELECTRONICS

The electronics can run in air at atmospheric pressure. The unit should be bolted to a heat sink. Without a heat sink the case temperature will rise continuously.

9.9 PULSER MODULES

Each pulser module consists of a high voltage power supply, DC conditioning, delay section and a pulser.

The power is supplied as combined RF and DC. Enabling a pulser involves switching a relay on the pulser card that connects the card to this supply. The DC is used to power the pulser and PFM identifiers and the delay confidence checking. The RF drives the high voltage supply for the pulser.

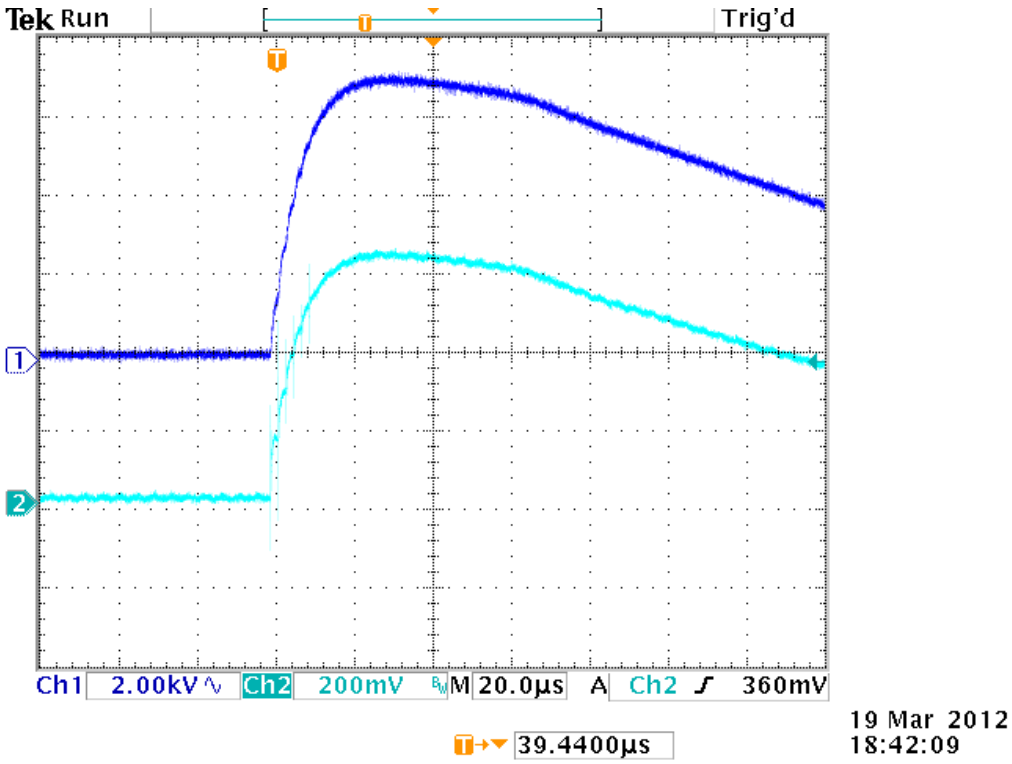


Figure 9 The phosphor pulse actual (dark blue) and monitor (pale blue).
The steps the pulse are due to the trigger to the Phosphor pulser. The phosphor pulser is repetitively triggered during the pulse rise to keep the IGBT switches on for ~ 40μs.

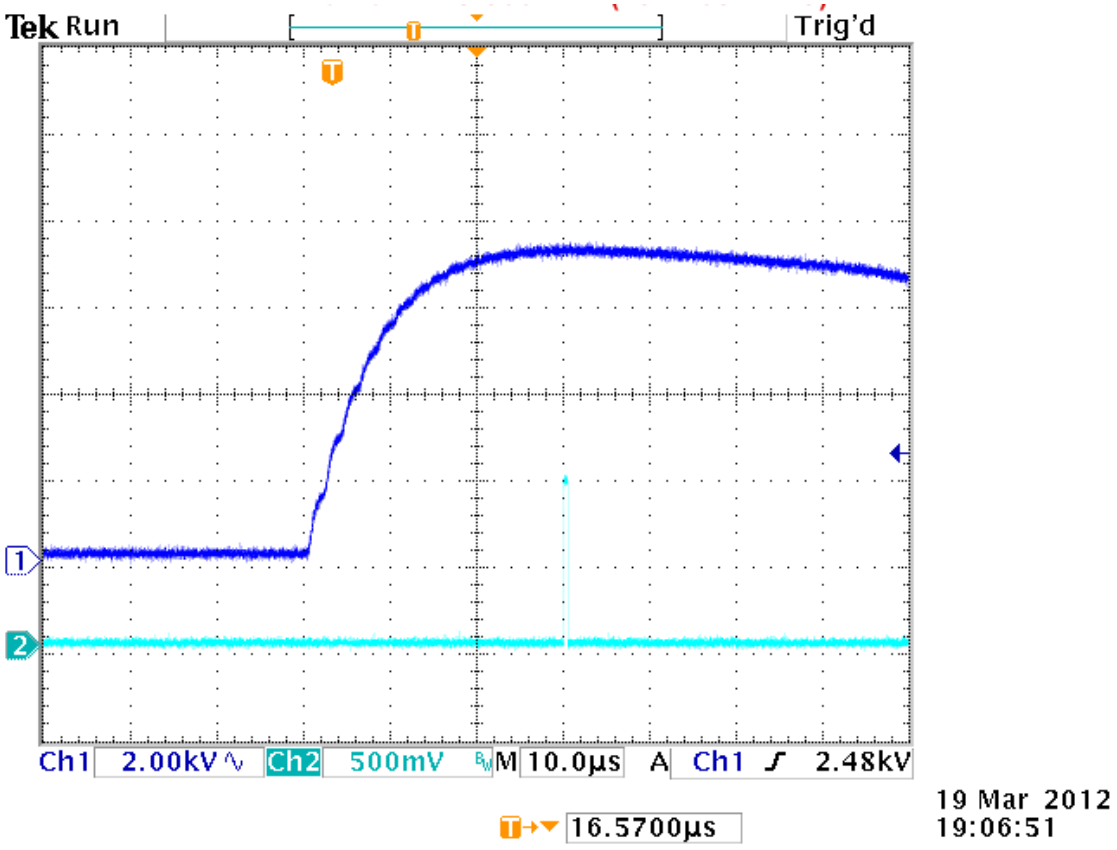


Figure 10 The fast gate sync. pulse and the phosphor pulse showing optimal cross timing of ~ 30μs

Control of the delay relays and the enable relay is via the 14 way backplane connector at the front of the pulser.

The delay works on a high level trigger pulse so that cross channel jitter is kept at a minimum. There is also a mechanical sliding trombone adjuster for each channel. Access to these is through a slot on the top of each pulser module. The slider allows up to 150ps of adjustment and is absolutely calibrated. The position should be clamped before use (although it can be slid during triggering when being set up). The clamp requires a 1.5mm AF hex key. The trigger leads from the trigger module are nominally the same length but are marked with the channel numbers for more accurate reproducibility of the delay settings.

As in the GXD there is confidence testing of the delay setting. This is achieved by injecting DC into the signal path, fitting resistors to ground on one half of each delay path. Measuring the voltage on the delay path then gives the number of delays "set". This is compared to the requested delay and then the relevant bit of the delay status register is set accordingly. Note that delay confidence needs the pulsers to be enabled in order to inject the DC into the delay path. The delay status register will not be updated unless the pulsers are enabled during a read back cycle. If the delays are changed with the pulsers disabled then the delay status register is not updated and will indicate the previous state. We recommend that the delay status is checked after the pulsers are enabled. In this way the user will have confidence in the delay just prior to using the pulsers.

9.10 PULSERS

The pulsers are of a design unique to Kentech and a detailed description of their working is not available to the user. However, some aspects of the design are available and may be required.

The drive pulse is generated using avalanche switches in a partial Marx configuration. This allows us the use of a low DC voltage of up to 4kV and yet generate much higher pulsed voltages. The basic pulser uses an array of 62 avalanche devices to generate a step voltage. This is fed into the output where a PFM is connected. The length of the pulse is determined by the components within the PFM.

9.11 CHANGING THE OUTPUT VOLTAGE

Unlike hGXD1 and 2, in hGXD3 there is the ability to switch the output voltage without dismantling the unit. The high voltage connection to the last output stack is controlled with a high voltage relay. This is controlled with a small slider switch on the top panel of each pulser. The relay is not rated to switch significant currents and so should only be changed when the RF power is not enabled. During the pulser enabling process (a write to the shift register and read back) the pulser enable relay state is changed enabling the 24 volt rail to be powered within the pulser and then the state of the high voltage relay is set according to the position of the slider switch. At the end of the read back cycle the RF power is turned on. This means that the high voltage relay never has to switch current at the high voltage, only block or pass the current.

Do not change the state of the slider switch whilst the RF power is enabled.

If unsure of the state of the RF, power execute a "safe" command or turn the unit off first.

The RF power can easily be switched on and off with the interlock connection on the front panel of the control unit. Do not use the RF power connection to disable the RF as this also disables the 24 volt supply and if they come on together the relay may have to switch significant current.

9.12 POSSIBLE OUTPUT WAVEFORMS

hGXD3 has been set up with 100ps PFMs to match, as near as is possible, those from earlier units. However, it is possible with little effort to make shorter gate pulses. In addition as the voltage control

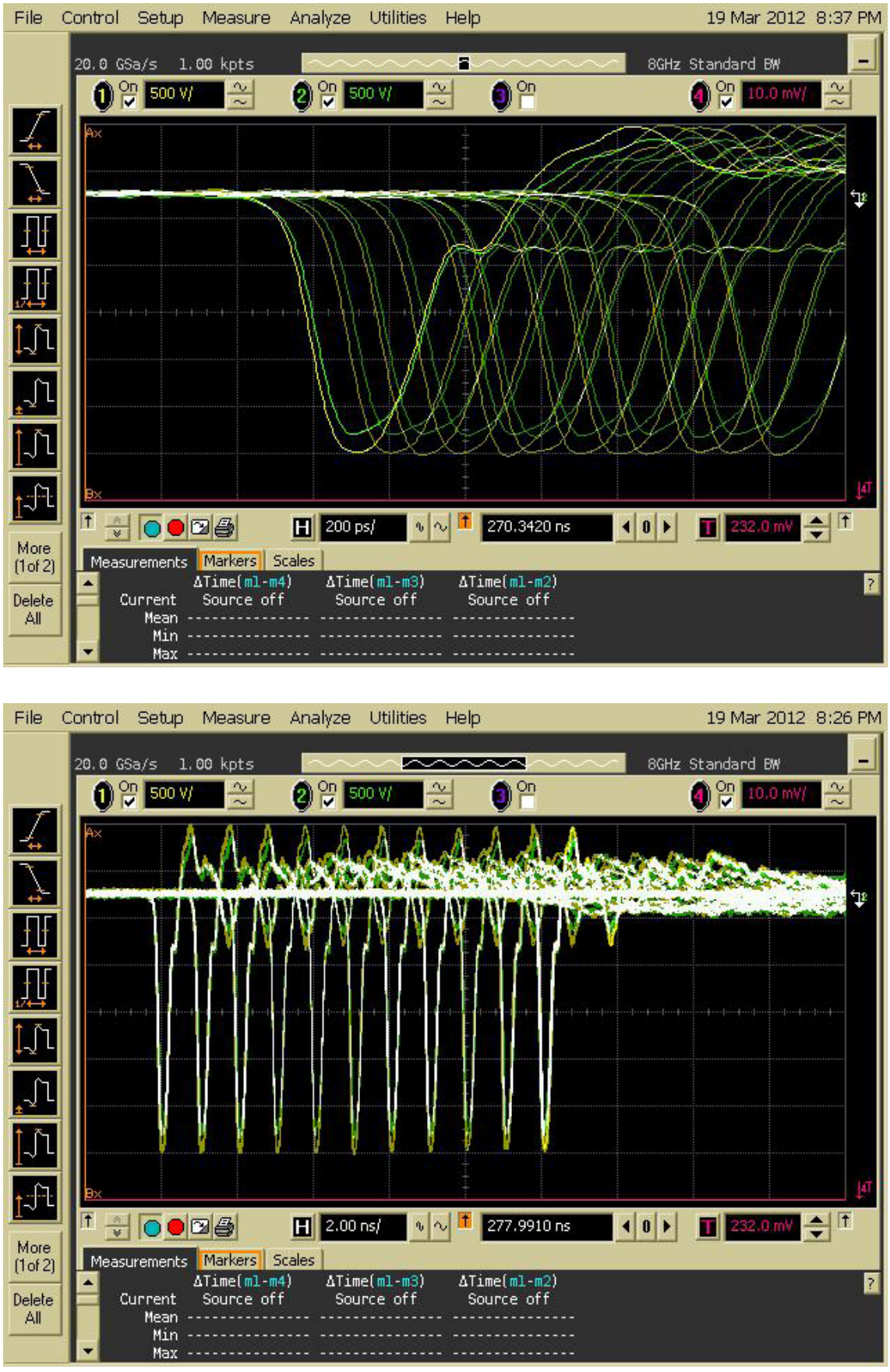


Figure 11 Checking the delays, above 100ps steps for channels 1 & 2, below 1ns steps. The two channels were made synchronous at the scope with the scope's skew function.

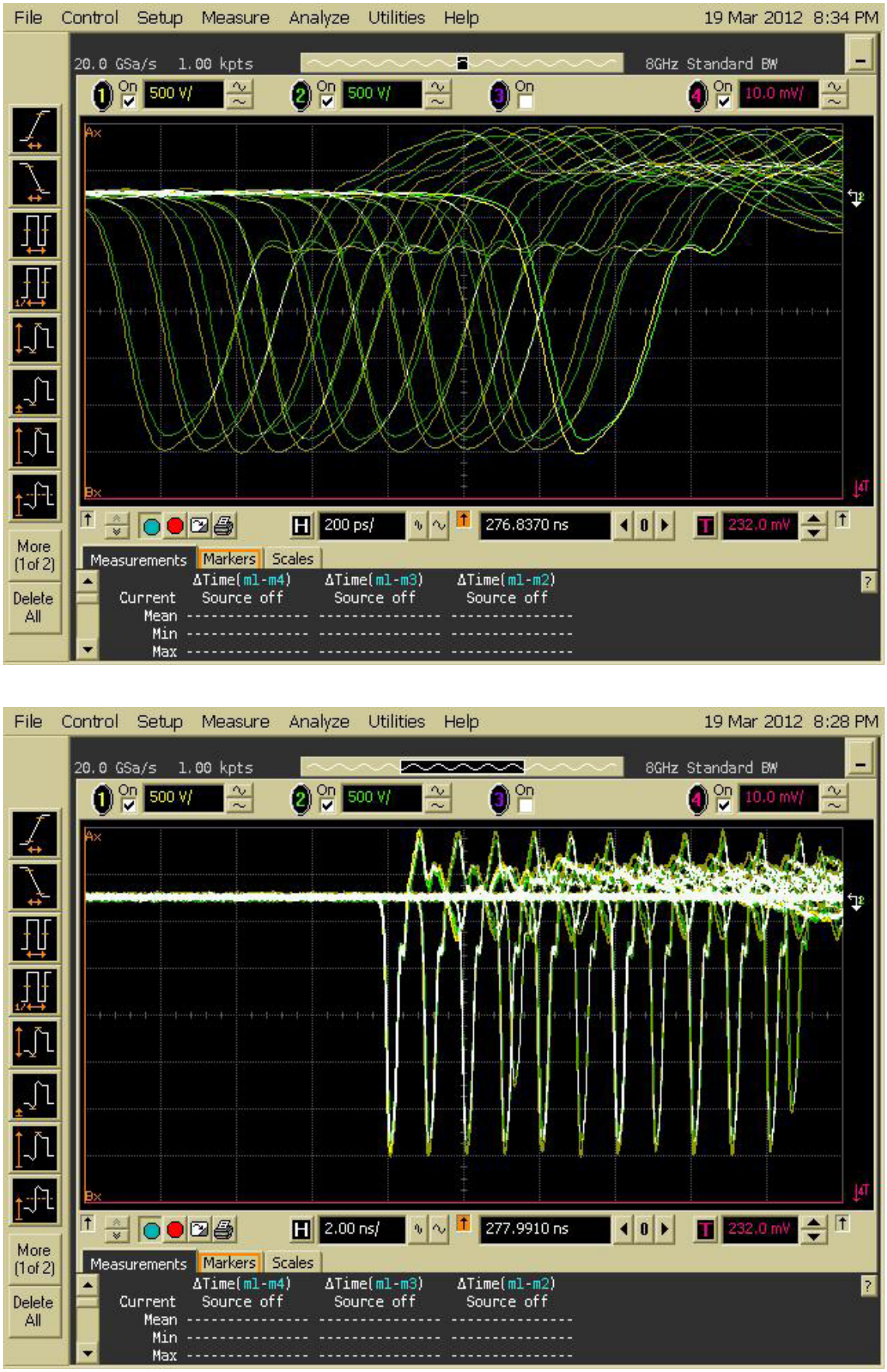


Figure 12 Checking the delays, above 100ps steps for channels 3 & 4, below 1ns steps. The two channels were made synchronous at the scope with the scope's skew function. The timing is as Figure 11. One can see the 6ns later arrival of ch3 w.r.t. ch1. The pulse sat far right are mis-triggers that occur as the RF power is turned off to set the delay

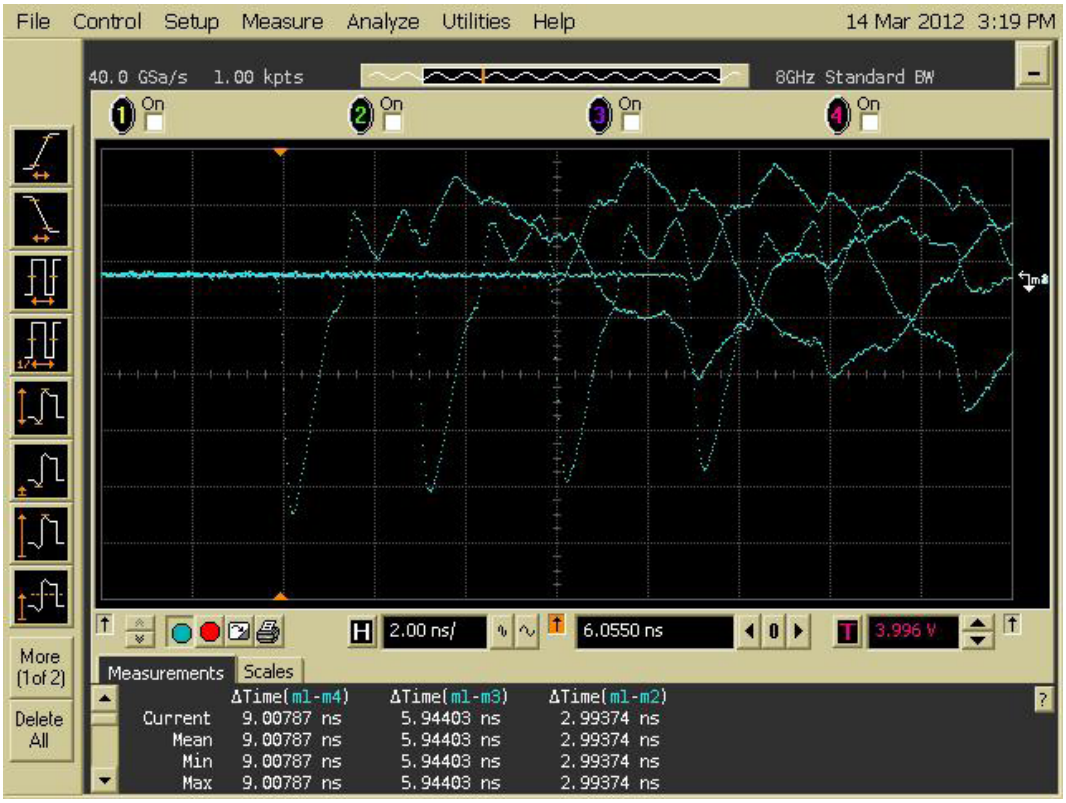


Figure 13 The trigger outputs from the trigger card showing staggering of the delays

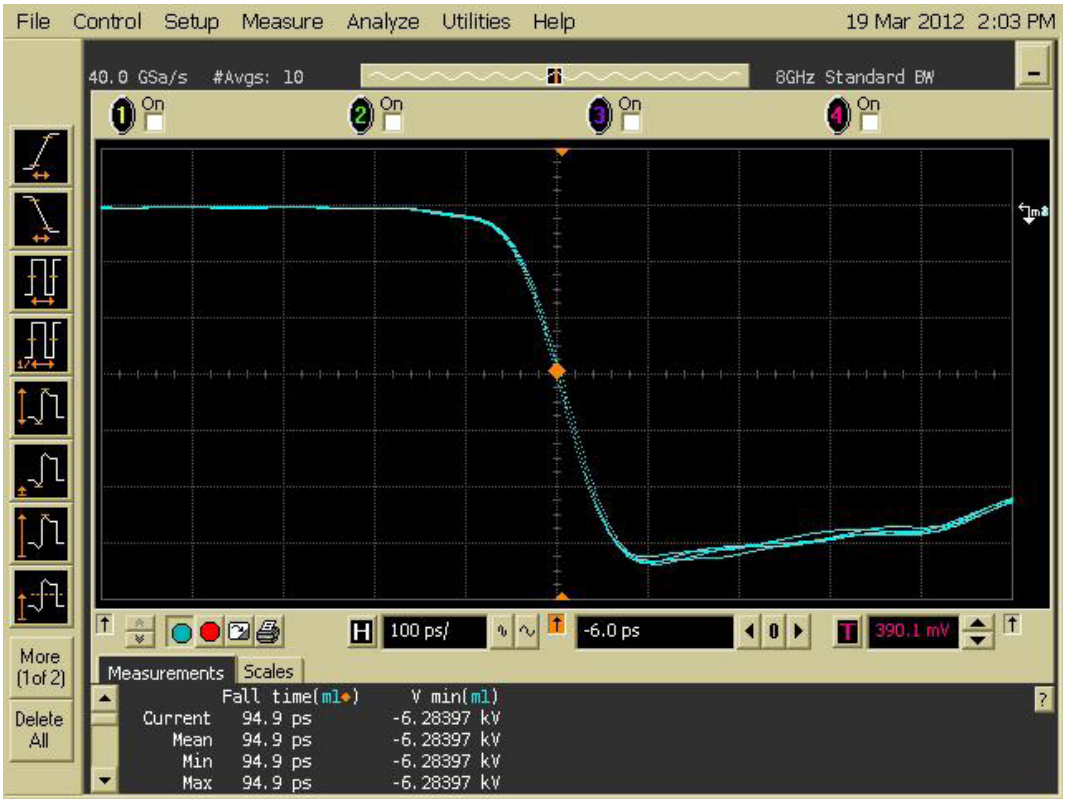


Figure 14 The 4 raw unformed outputs from the pulsers superimposed.
The channels were delayed 9, 6, 3 & 0 ns for Chs 1 through 4 respectively. In addition the fine delays were set to 30, 47, 26, 0 ps for Chs 1 through 4 respectively.

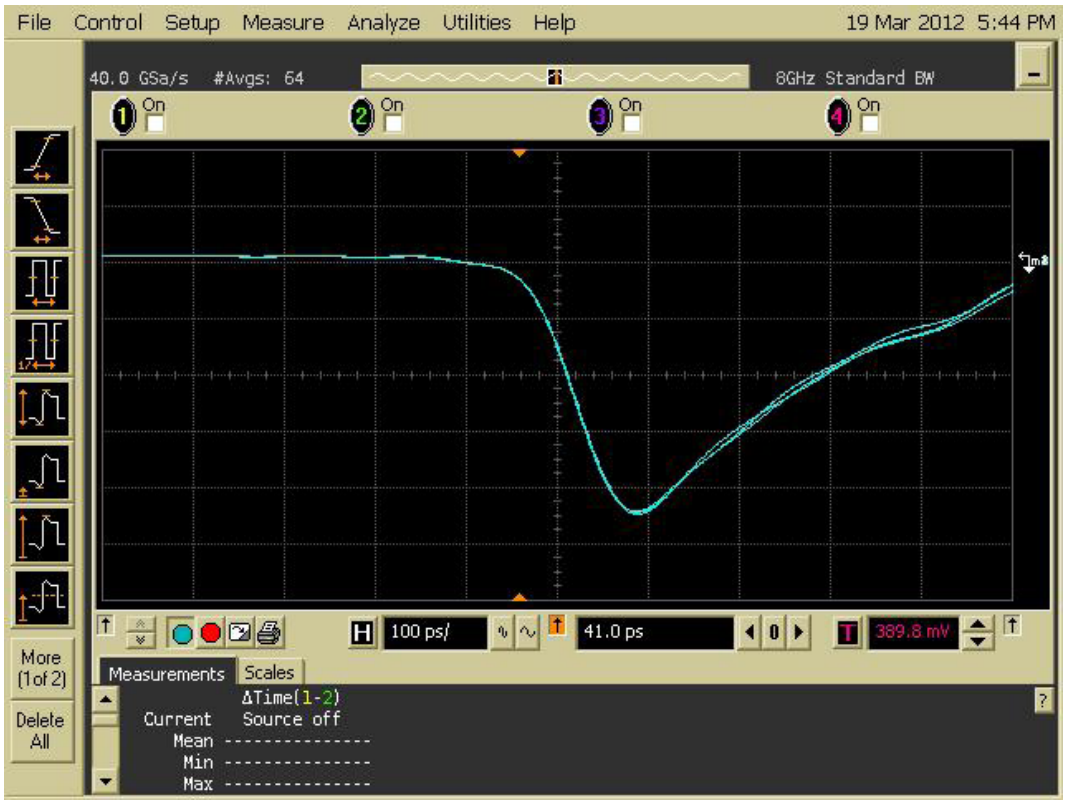


Figure 15 Main Gate output pulse waveforms 4 x 100ps modules superimposed. High voltage setting. Peak is at is -4530 volts.

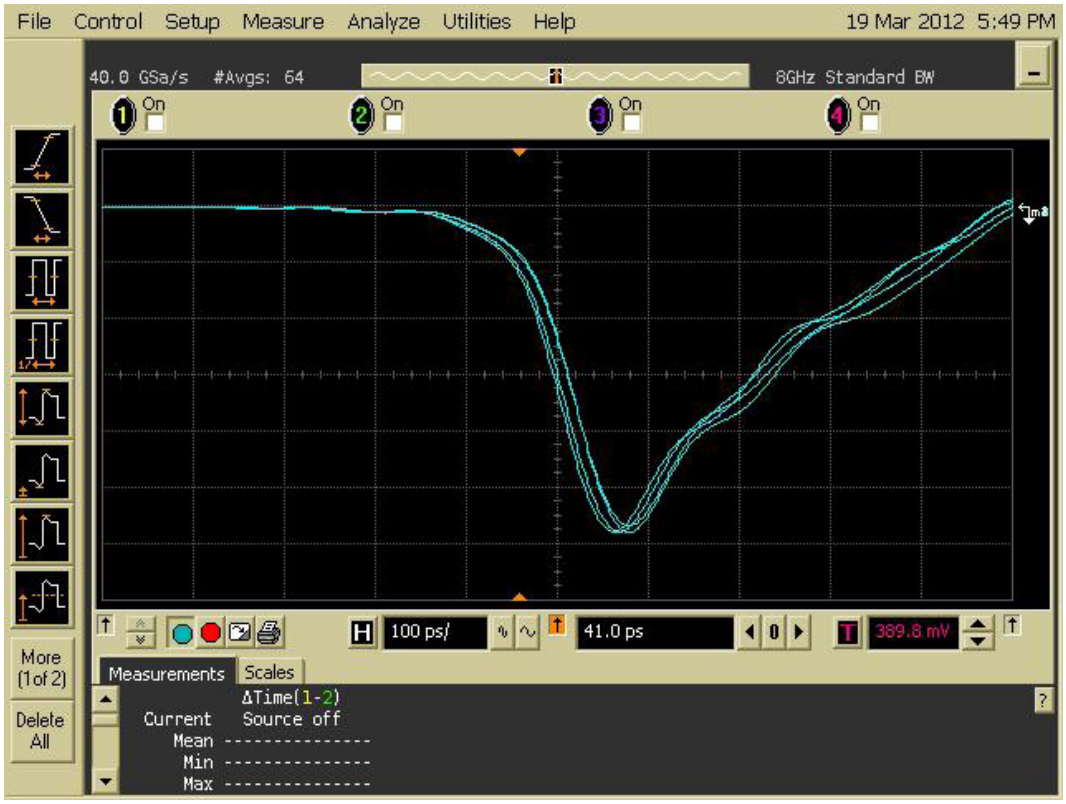


Figure 16 Main gate output pulse wave forms 4 x 100ps modules showing relative timing. Low voltage output. PRM timing differences are shown for synchronised raw pulses. Peak voltage ~ 2.8kV

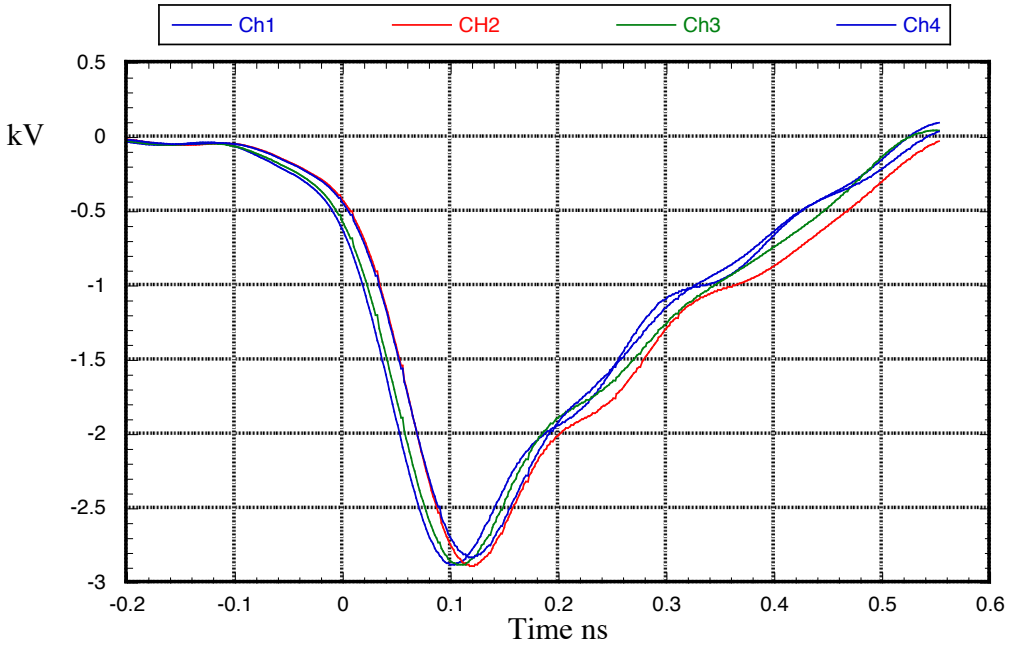


Figure 17 As Figure 16 on page 24 but with scales.

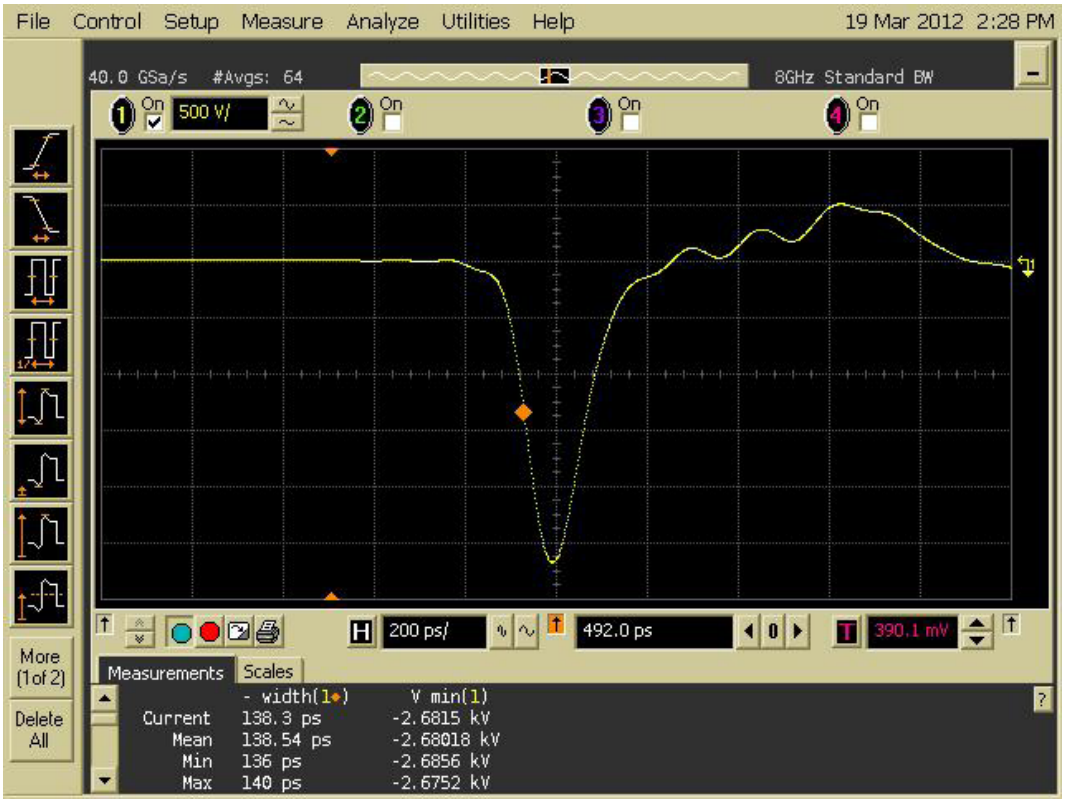


Figure 18 Waveforms that can be achieved with simple changes.

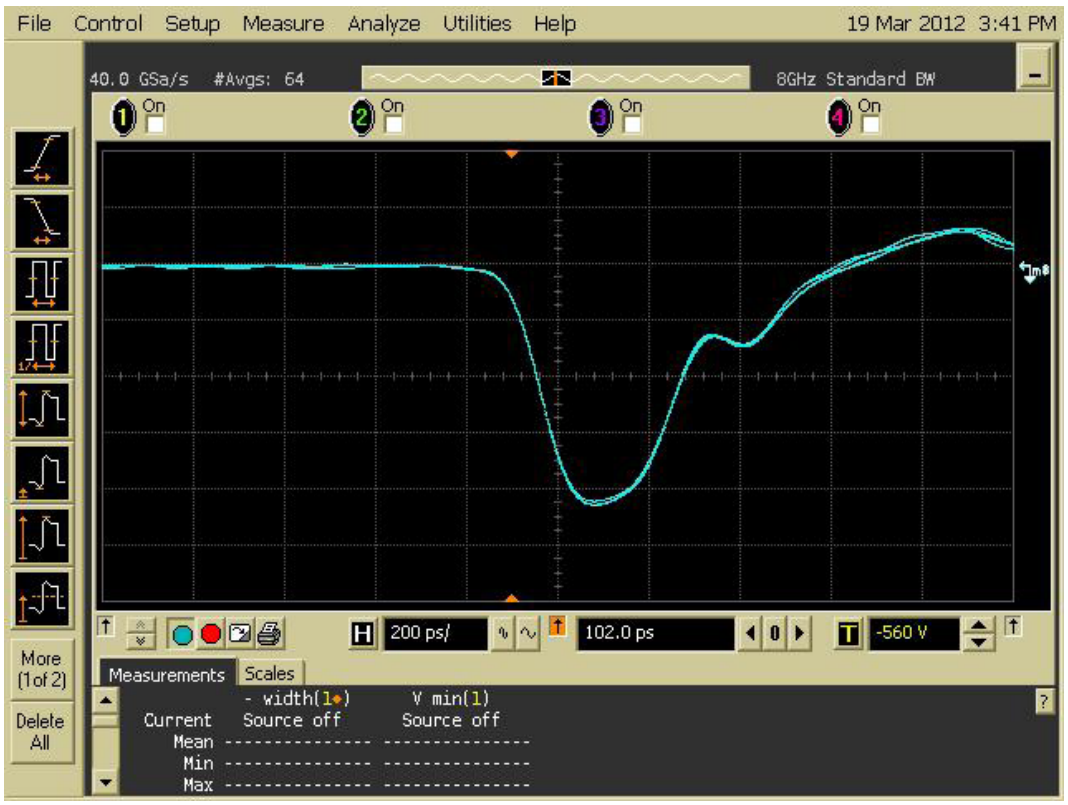


Figure 19 Main Gate output pulse waveforms 4 x 200ps modules superimposed.

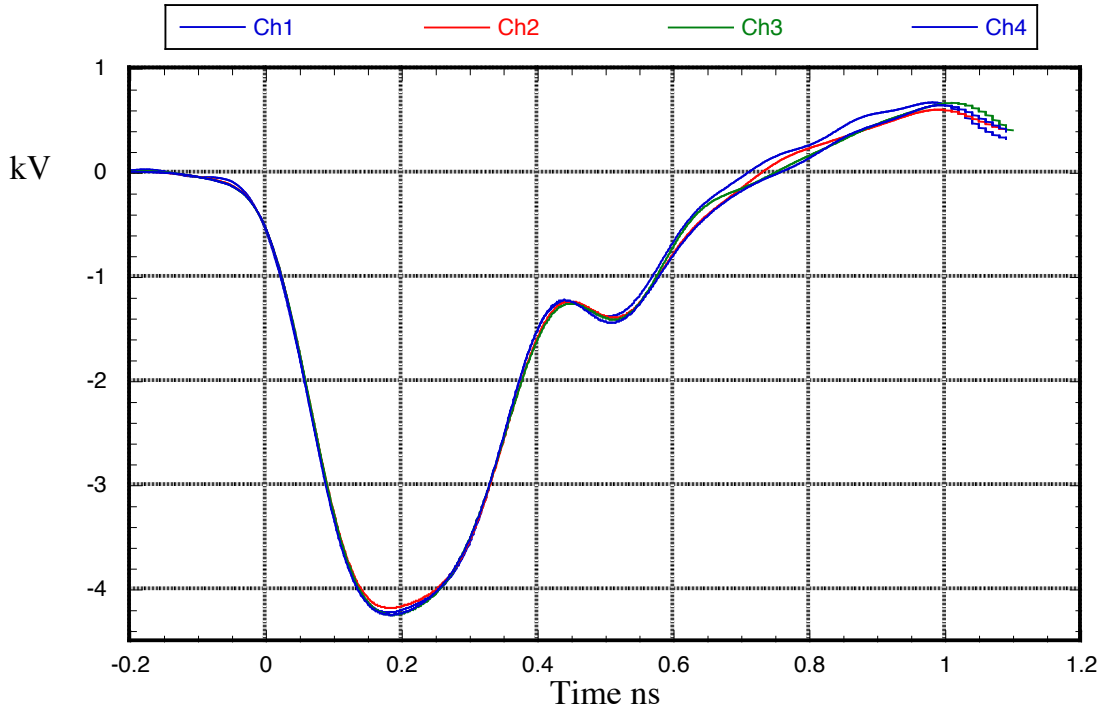


Figure 20 As Figure 19 but with scales.

Figure 21 Main Gate output pulse waveforms 4 x 400ps modules superimposed

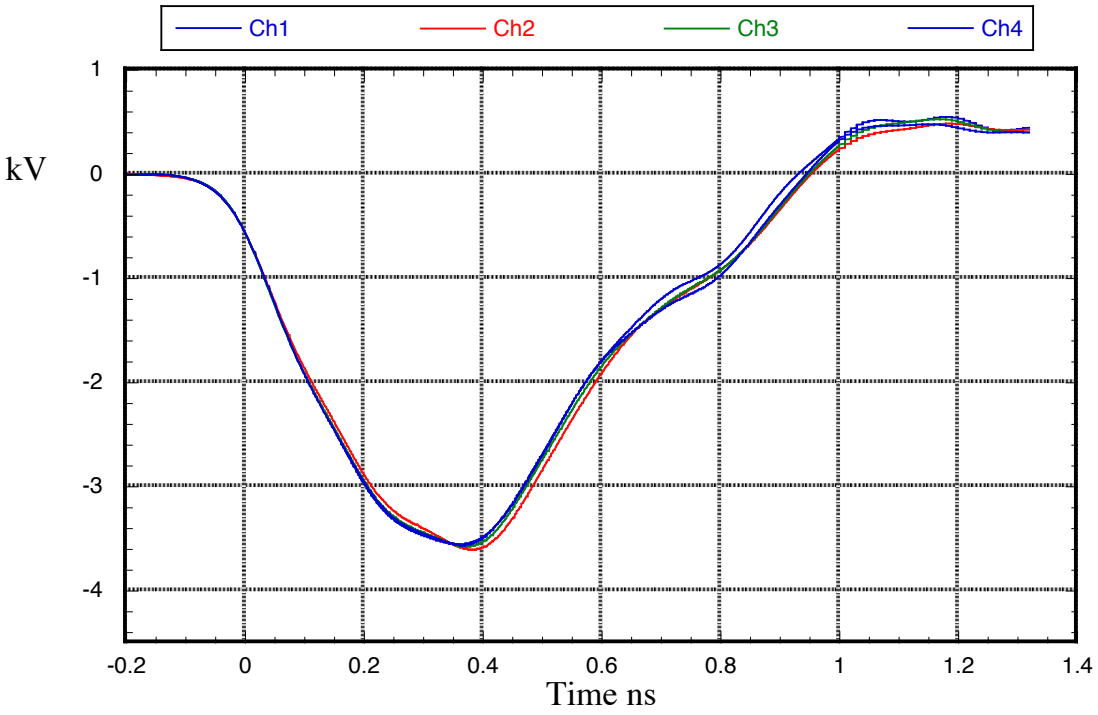


Figure 22 As Figure 21 but with scales

is now readily available it would be possible to switch to the higher voltage when changing to the shortest pulses, so compensating for their normal reduced output.

Some waveforms are shown in Figure 18 on page 25

The 100ps PFMs use a short length of thin wire to provide a defined inductance to ground. This differentiates the raw waveform, turning a step into a short pulse. Adjusting the length and shape of the wire loop to ground adjusts the pulse length. It is a simple matter to set up new short waveforms.

Thin wire is desirable as one can obtain a significant inductance in a short length. The length has to be ~< the required pulse length x the speed of light and the inductance ~ 2.5nH.

9.13 TRIGGER MODULE

The trigger module consists of a high voltage power supply, a trigger pulser, trigger amplifier, second trigger amplifier, pulse conditioning, pulse transformer, pulse splitter and staggered delay cables.

There is a single relay for enabling the unit driven from the backplane connector.

The trigger circuit is designed to be triggered from the control unit and its sensitivity is set to be suitable for this. If it needs to be triggered directly for testing a fast rising (<2ns) long (~100ns) 30 volt pulse (into 50Ω) should be used.

The outputs of the trigger module are staggered with approximately 3ns between outputs, see Figure 10 on page 19.

9.14 BIAS SUPPLIES

Each of the four bias supplies (in the comms. unit) can deliver from -950 to +950 volts. The supply works in the following manner. The supplied RF is transformed and rectified to deliver ~ + and -2.5kV. The polarity is selected with a high voltage relay. The output is fed to a zener chain with relays across zeners. Activating the relays shorts out zener diodes and reduces the output voltage. Note that maximum power is consumed at zero voltage output. The stability of this arrangement is not as good as GXD. Calibrations are shown in Figure 23 on page 29 and Figure 24 on page 30.

9.15 PHOSPHOR PULSER PERFORMANCE

The phosphor circuit can deliver DC output up to ~ 3kV or pulsed, up to ~ 10kV.

The actual value depends both on the voltage setting and on the load. There is provision to feed back a connection from the phosphor to the unit to check for continuity. This will load the circuit and reduce the DC performance. In pulsed mode it adds about 25pF to the capacitive load.

The phosphor circuit uses a 4 stage Mark generator to deliver the pulse. This enables significantly more volts to be available in pulsed mode. IGBT switches are used in the Marx generator. The pulser switches a local series stack of capacitors into the output connection. The actual voltage that appears at the output depends upon the load capacitance. The charge stored internally must be shared between the internal capacitors and the output capacitance. The internal capacitance is ~ 3.8nF. Low capacitance cable should be used to the phosphor if the load is long. The cables provided are 75Ω, RG179, which is about $63pFm^{-1}$.

The expected output will be

$$V_{out} = V_{set} \times 10/3 \times 1/(1+C_{ld}/C_{in})$$

Where V_{set} is the set voltage, V_{out} is the expected output voltage, C_{ld} is the load capacitance including the out and return cables and the monitor and C_{in} is the internal capacitance. The 10/3 factor comes from the Marx gain. V_{set} can be up to 3kV, C_{in} ~ 3.8nF

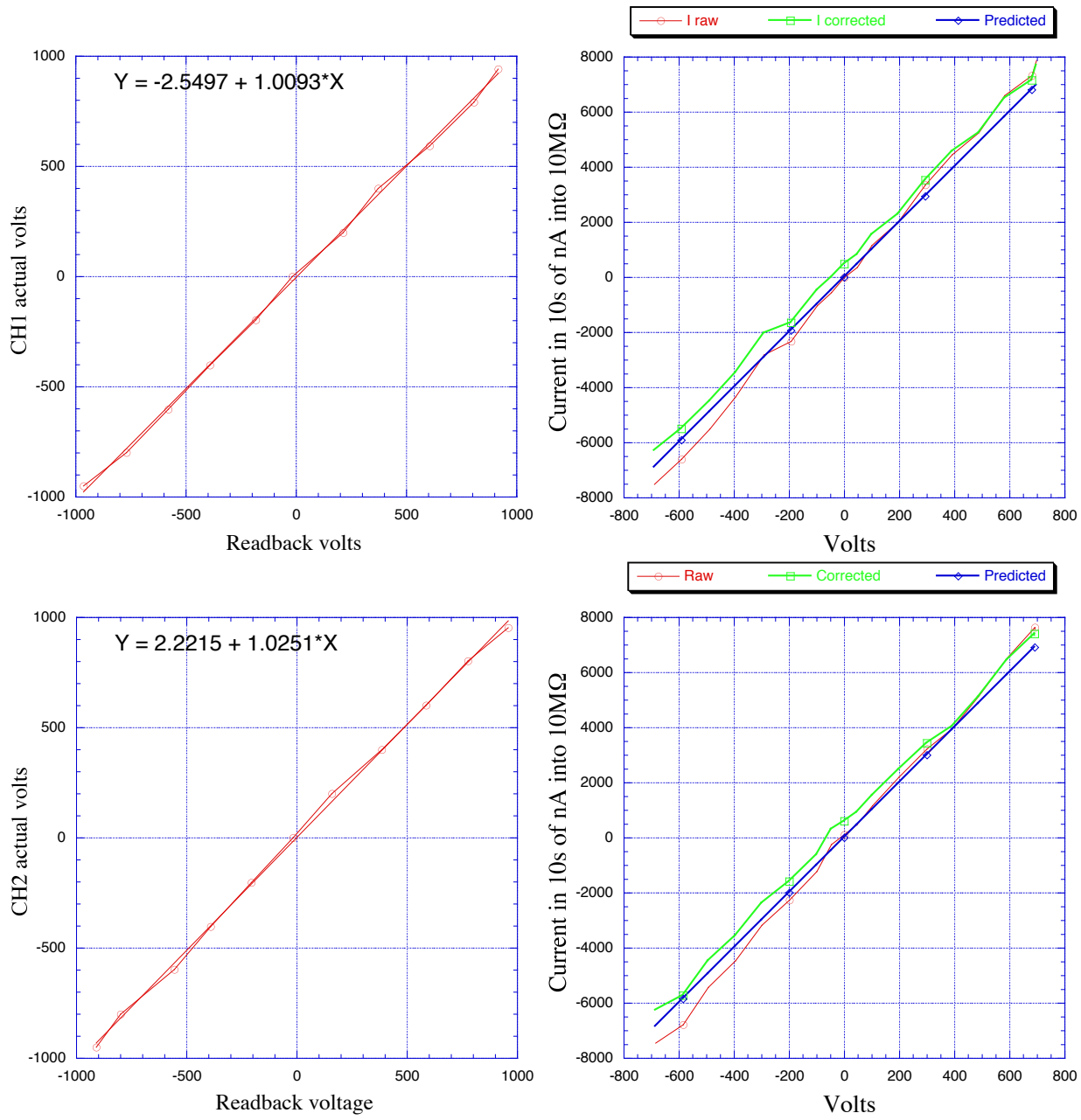


Figure 23 Voltage (left) and current (right) calibrations for channels 1 (top) and 2 (bottom)

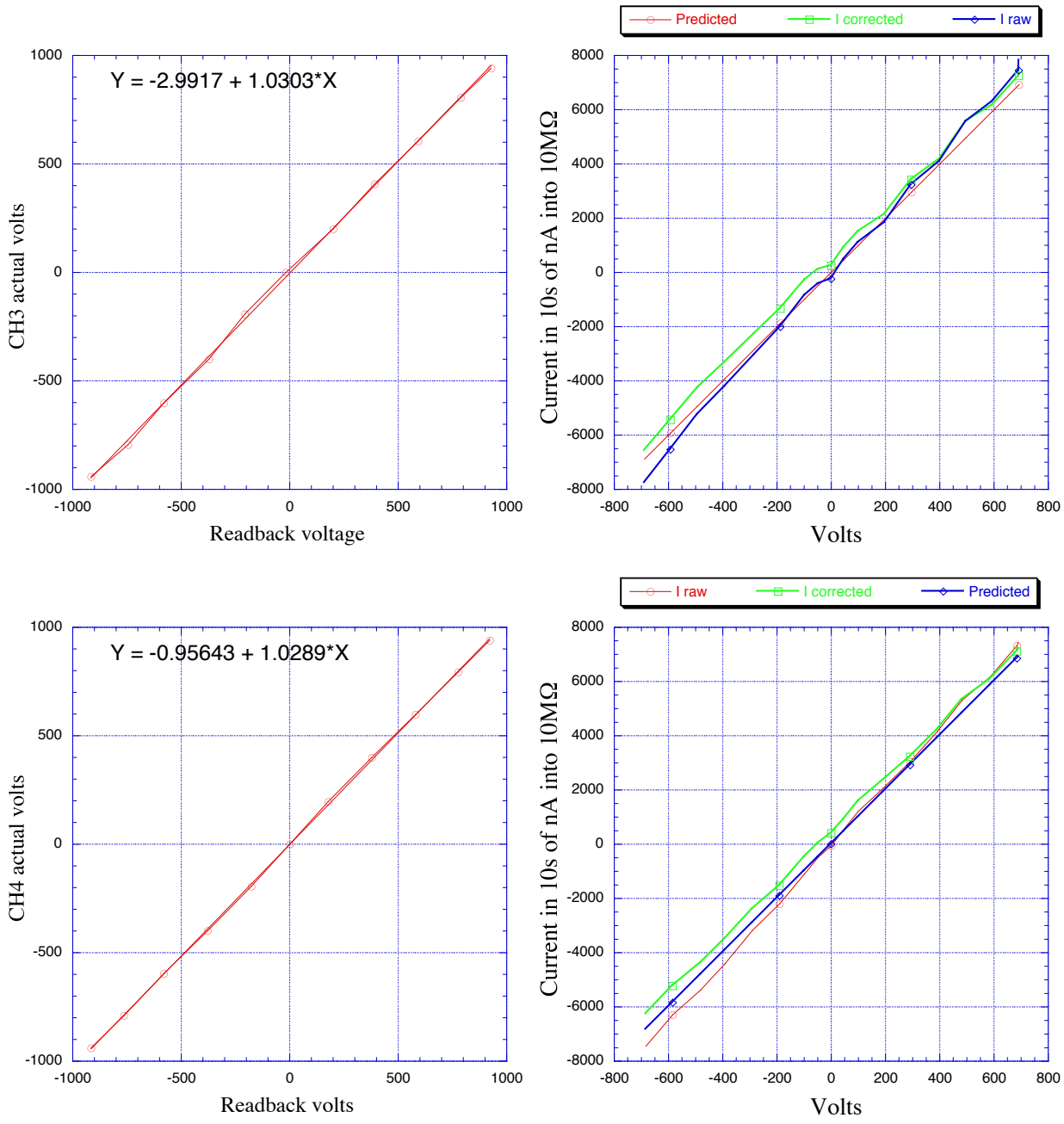


Figure 24 Voltage (left) and current (right) calibrations for channels 3 (top) and 4 (bottom)

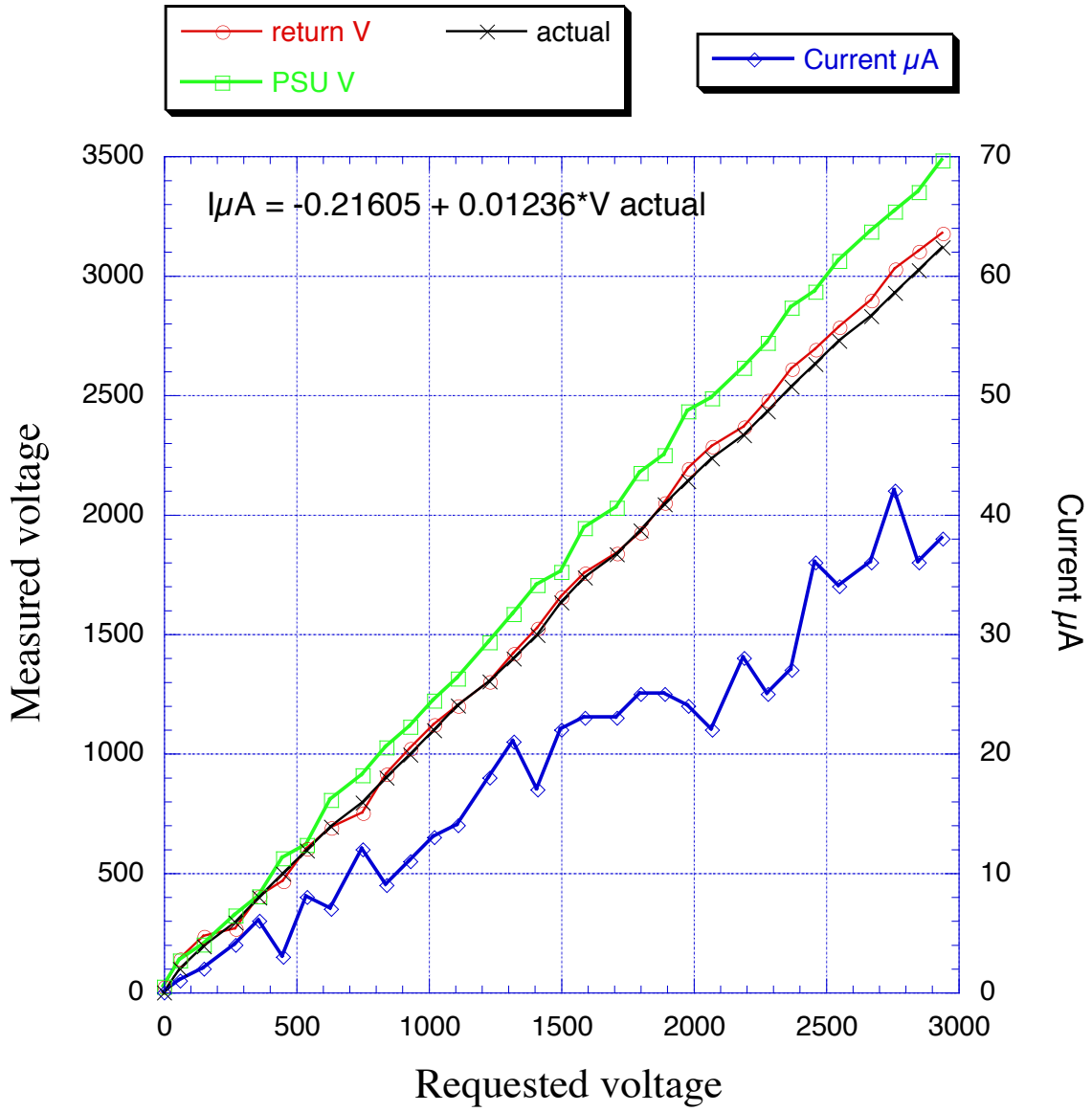


Figure 25 The DC phosphor calibration for voltage and current (into 1GΩ)

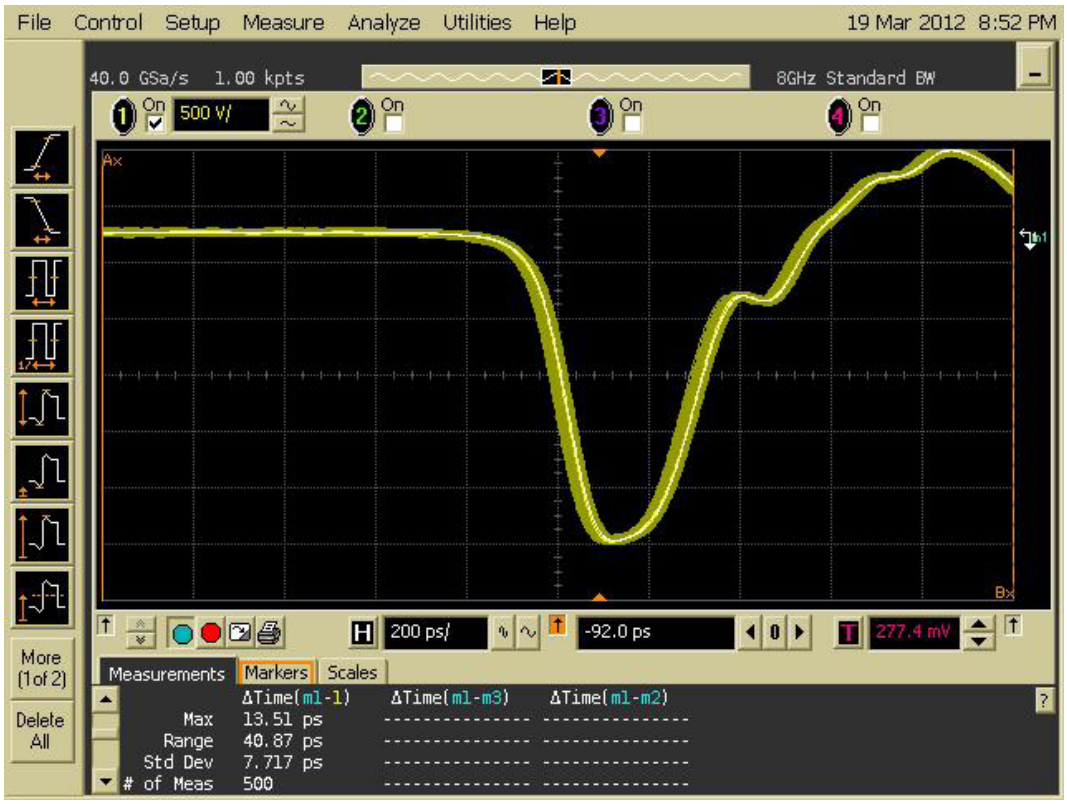


Figure 26 The overall system jitter when driven optically
Range 40.87ps, SD 7.717ps

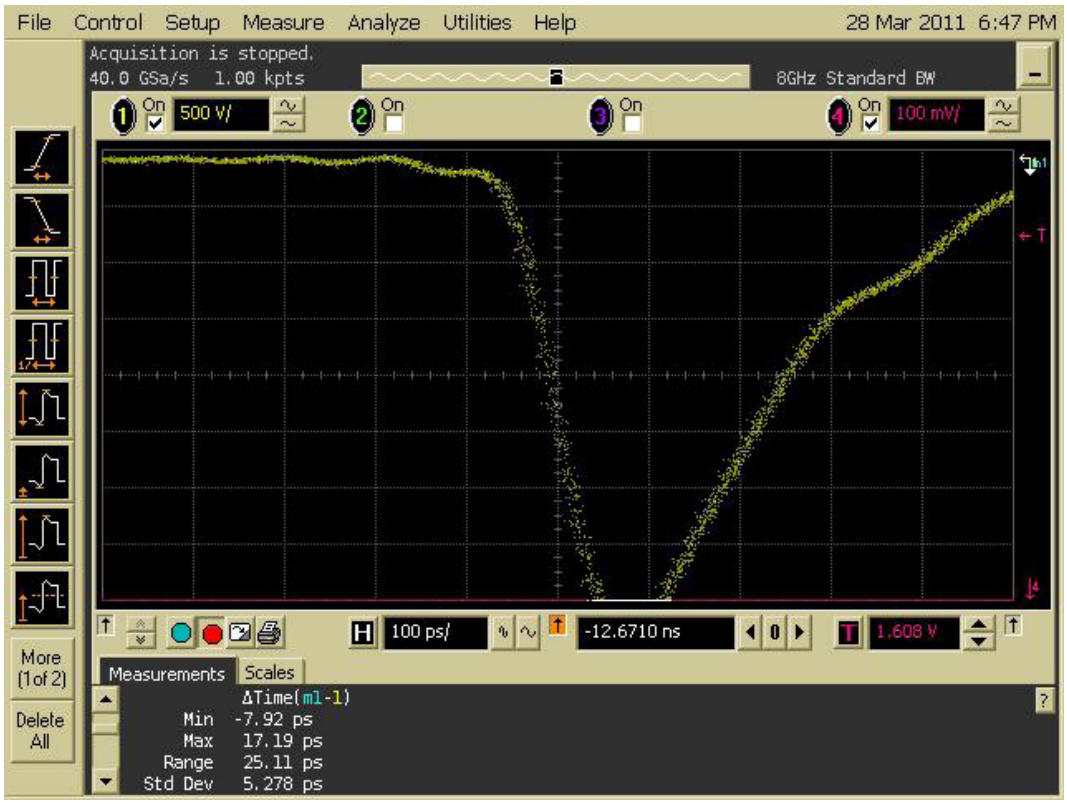
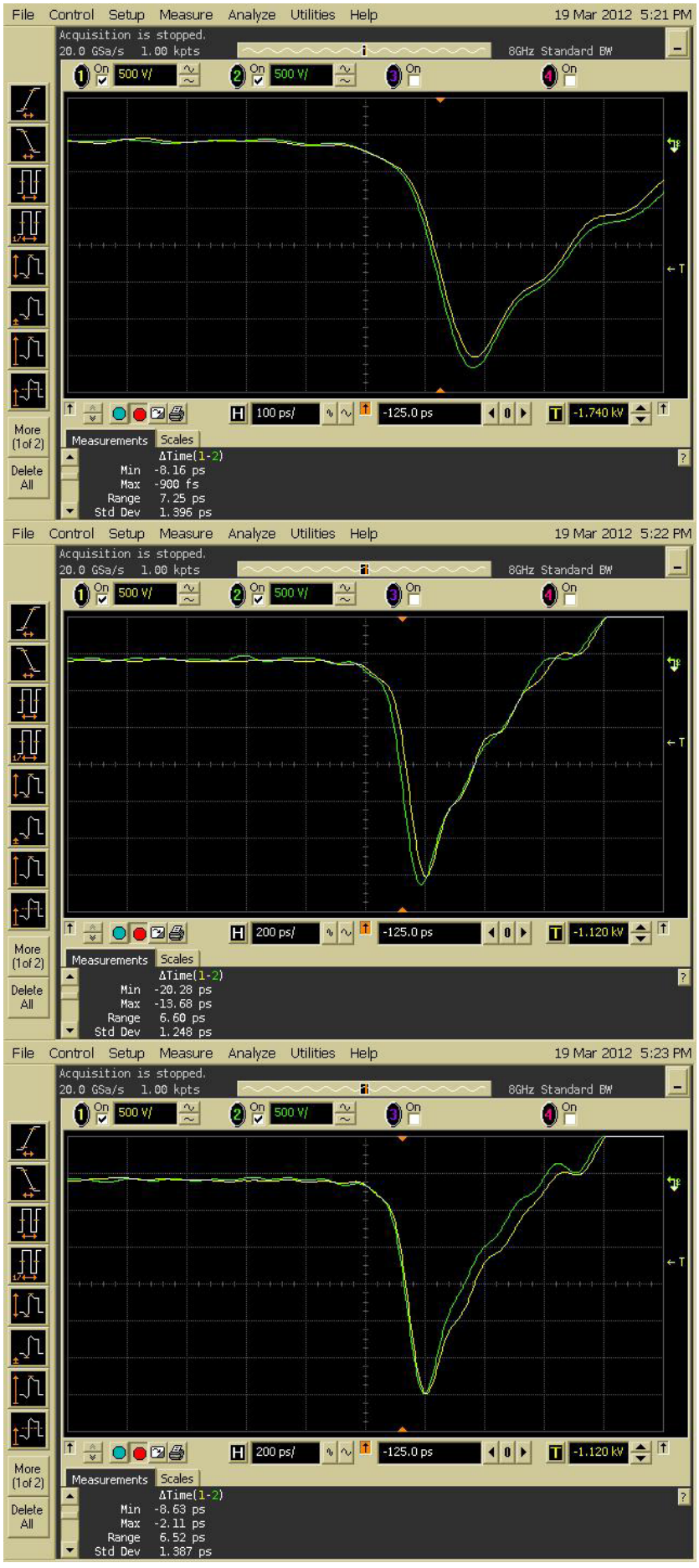


Figure 27 The overall system jitter when driven electrically
Range 25.11ps SD 5.278ps



Channel 1 to 2 jitter.

Range 7.25ps SD 1.396 ps

Channel 1 to 3 jitter.

Range 6.6 ps SD 1.248 ps

Channel 1 to 4 jitter.

Range 6.52 ps SD 1.387 ps

Figure 28 Channel to channel jitter

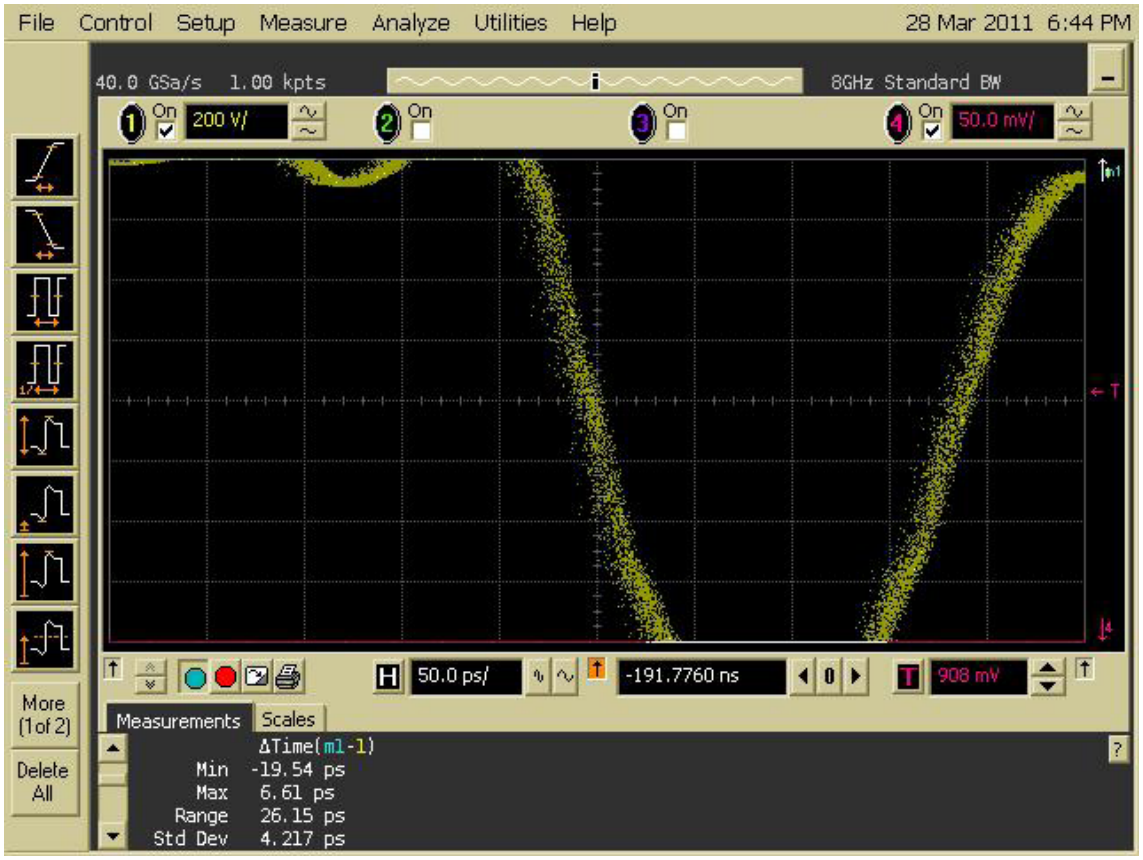


Figure 29 The overall system jitter with the head driven directly.

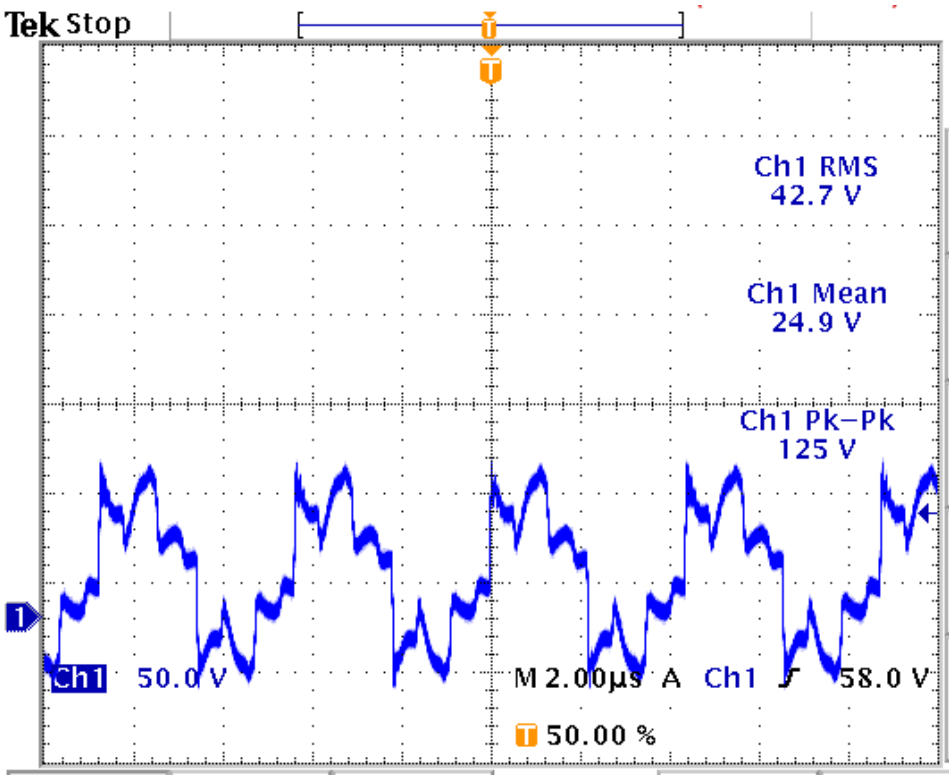


Figure 30 RF power waveform

If the feedback connection is made the user has the ability to measure the voltage on the phosphor in DC mode and hence to check continuity. This can be performed by the hGXD (as in GXD) or separately with the external monitor fitted to the rear of the head. On GXD the monitor was amplified and combined with the pulse monitors, on hGXD it is separate and has no amplifier. Pulsed waveforms seen on the monitor are more representative in shape but also pick up the RF drive and the trigger pulses, see Figure 9 on page 19.

9.16 THERMISTOR

There is only one thermistor on hGXD. For compatibility with GXD software, the same commands are used and the sensor should be numbered in the range 0 through 16, however, the same thermistor value is always returned.

If the temperature is requested during a write or read cycle the returned value is the last one obtained.

At other times the temperature is read from the head in real time. The shift register has a quiescent state and this is used for the temperature monitoring. This is why the temperature and only this parameter, is the current value except when a read or write cycle is in operation.

9.16.1 THERMISTOR POSITION

The thermistor is fitted to the comms 2 board in the comms module. It is placed over some zener diodes in the bias supply as these seem to get the hottest. Temperatures to 60°C are not unexpected. The relays that select the bias polarity are astable and one per bias channel is always active. These are responsible for quite a lot of the heating observed. This is independent of the voltage or enable settings.

9.17 CONTROL UNIT

The CU contains the interface to the outside world, the μProcessor, the RF power supply and the two trigger channels are all controlled here locally.

All connections to the head unit are via the rear panel. Connections to the outside world are via the front panel.

9.18 PHOSPHOR TRIGGER CIRCUIT

This accepts electrical or optical input. If electrical it should be <5 volts.

The jitter in this circuit is adequate for purpose. Note that the phosphor should be triggered earlier than the main trigger by about 38μs.

9.19 RF POWER TRIP

There is a trip on the RF power sent to the head. The trip level is set with a potentiometer in the control unit. There is no software control over this. Once tripped, it can be reset with the "**safe**" command. Note that this will disable the pulsers, the phosphor and the biases. Consequently the RF power will end up enabled but the power level set to zero as there will be no load.

When the RF power trips the Comms light on the front panel of the control unit will flash at 1Hz, see section 9.21 on page 36.

9.20 RF DISABLE ON TRIGGER

By setting bit 11 in the control register to a 1 the user can enable the "disable RF power on receipt of a fast trigger" feature. This feature uses the fast trigger detect circuit to shut down the RF, so it

is also necessary to enable the fast trigger circuit, bit 9 of the control register. Normally one would have everything enabled.

Once a fast trigger is detected the RF is shut down and bit 14 of the control register is set to 1. To turn the RF power back on requires a 1 to be written to bit 15 of the control register, or the feature to be disabled by writing 0 to bit 11 of the control register.

The state of the RF can be monitored in the enable register, bits 1 and 2.

9.21 LEDS

There are no LEDs on the head unit. There are a few inside that help diagnosing shift register issues should they arise. There are 4 LEDs on the front panel of the control unit. They have the following behaviour.

Table 1 LED indicators

LED	Position	Notes
1	Above fast trigger input	This is quiescently ON in optical trigger mode and blinks OFF when triggered. It is quiescently OFF in electrical trigger mode and blinks ON when triggered.
2	Above phosphor trigger input	As above
3	Above Interlock	LED illuminated when interlock is broken.***
4	Comms	LED can be ON, OFF or Flashing @ 1Hz.*

* The Comms LED has the following behaviour:

Table 2 Comms. LED meanings

LED State		Meaning	State of RF power to Head
ON		"RF disable on trigger" is set and a fast trigger has been received	OFF
OFF	1	"RF disable on trigger" is set and no fast trigger has been received and the RF power has not tripped.	Logically ON**
	2	"RF disable on trigger" is not set and the RF power has not tripped.	Logically ON**
Flashing @ 1Hz		The RF power has tripped.	OFF

** "RF Logically ON" means that the actual power level depends upon what is enabled at the head. If nothing is enabled the power is logically ON but the power level is set to zero.

*** The behaviour of the Interlock and Comms LEDs can be reversed in software with "debug " level commands.

9.22 PULSE FORMING MODULES

The pulse forming modules fit to the front of each pulser module. The PFMs are each unique and can be identified by the software by way of three resistors connected internally to a small 4 way plug on each module. The resistor values for the supplied PFMs are shown in section 13.2 on page 62. If we supply further modules the resistor codes will be continued as per this appendix. Note that the software does not identify the module, it only reads the resistors, it is up to the UCS to translate this into module ID. The appendix can be provided in electronic form for direct use in the UCS.

9.23 PHOSPHOR TRIP CURRENT

hGXD has no Phosphor current trip. The current trip commands from GXD are accepted but do nothing.

9.24 OPTO TRIGGER THRESHOLD

The opto trigger threshold is not adjustable, however, the user could replace resistors around the front end of the trigger circuit but should seek advice from Kentech Instruments before proceeding.

9.25 MAIN OUTPUT PERFORMANCE

9.25.1 MAIN OUTPUTS

The main outputs are approximately 6kV into 50Ω. They should not be run into open circuits as the output TNC connectors cannot take the high voltages produced. Repeated breakdown at the connectors is likely to erode the insulator. If only one oscilloscope channel is available for testing then the other channels should be switched off or terminated with leads to move the breakdown away from the connector.

The main output voltage can be reduced to about 4kV by disconnecting the charging resistors to the output stack, see section 12.1 on page 37.

9.25.2 JITTER

Figure 26 through Figure 24 show jitter measurements. Whilst system jitter is not exceptional, channel to channel jitter is significantly better than GXD units. The overall system jitter measurements were made from the front panel of the Control unit through 50m of LMR600 cable connecting the control unit to the head.

9.25.3 CHANNEL SYNCHRONISATION

The raw outputs have been synchronised by adjusting the fine delay with the coarse delays set to 9ns, 6ns, 3ns, 0 on channels 1 through 4. Figure 16 on page 24 shows the channel synchronisation with the 100ps PFMs fitted. The internal delay in these PFMs is not quite the same.

9.26 SERIAL NUMBERS

Unlike GXD serial numbers of the modules are not complex encodes of the Kentech job number. Instead simple coding is used similar to that used for the pulse forming modules. The pulsers are identified internally so that the correct delay calibration data is used and pulser modules can be placed in any of the four pulser slots; the software will apply the correct delay data. The comms. module serial number will be read as a simple number as in the table blow:

Table 3 Unit numbers to serial numbers

Unit number	Job number
as returned by @cs#	Unit serial number
1	J1007081
2	J1010221
3	J1109123
4	J1109124

9.27 MODULE ID NUMBERS

Module ID numbers are used internally to identify delay data. Initially it was thought that the control unit would know about the delay data of all hGXDs and load the relevant delay data. This has not

been implemented. Instead the system checks to see which pulser module is in which slot on the back plane and uses the relevant delay data for the module.

If channel 1 is in the left most slot (then 2,3 and 4) looking onto the output of the head then the command **n @mid** will return the following values for hGXD3 (J1109123) and hGXD4 (J1109124):

n	**n @mid** response J1109123	**n @mid** response J1109124
0	3	4
1	31	41
2	32	42
3	33	43
4	34	44

If modules are not in the relevant slots the system identifies where they are.

10 MAINTENANCE

The unit should require little maintenance. The only possible exception is lubrication of the PFN screw threads. The software can be upgraded over the RS232 link, see section 12.1 on page 56.

10.1 DISMANTLING THE MODULES

The unit is simply split into its modules with the following procedure:-

1. Remove the PFMs
2. Remove all leads including the trigger to pulser trigger leads on the rear panel
3. Remove the lower rear strap that attaches the pulser and trigger modules to the comms module, (6 M3 cap heads and 2 M2 cap heads)
4. Ease the pulser and trigger module as a single lump back from the backplane panel of the comms module.
5. Remove the rear top strap across the pulser and trigger modules, (5 M3 cap heads)
6. Remove the front strap from across the pulser and trigger modules, (5 M2 pozidrive screws)

10.2 RE ASSEMBLING THE UNIT

Just reverse the above instructions but note that the trigger module can only be fitted to the central slot on the backplane. The pulser modules can go in any of the four other positions.

The trigger outputs from the trigger module are staggered at approximately 3 ns intervals, 0,3,6,9 ns. The trigger delay of the pulser modules are all similar. The fine delays have been set assuming that trigger 1 goes to pulser 1 with trigger lead 1, etc.

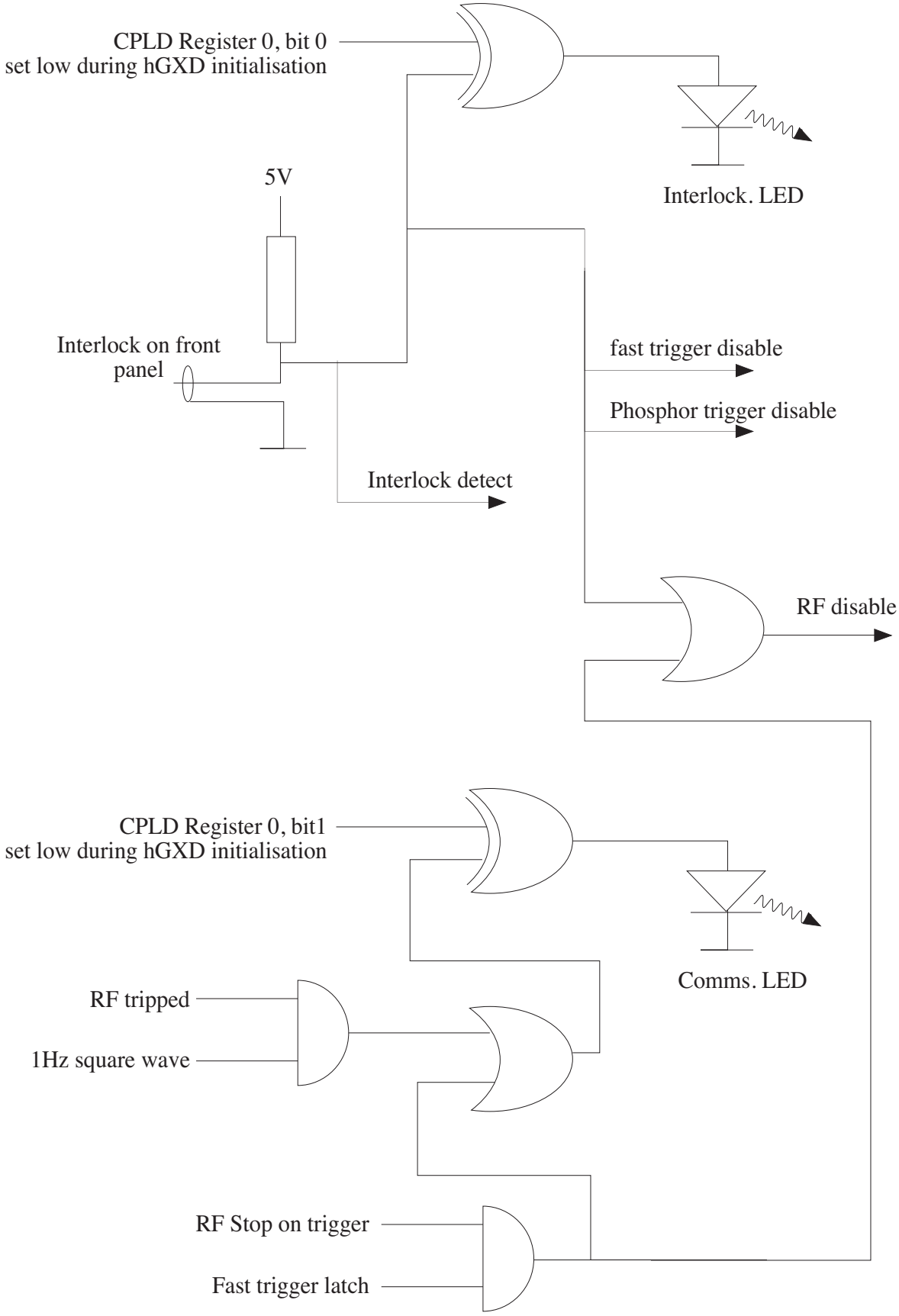


Figure 31 Interlock Logic

11 hGXD SOFTWARE INTERFACE

11.1 REVISIONS

V34 This version fixes bugs in V32 associated with compensating for the significant currents in the ground connection between the head and the control unit. There is no longer an empirical correction. V34 should be able to replace V32 in hGXDs 1 and 2 (but not the unit with the module ID fault).

V33 a special version of V32 with the module ID system over-ridden. This was to overcome a connection issue with the module ID resistors in hGXD1 or 2.

With this version of the software it is important to fit the modules in the correct slots. Looking onto the output channel 1 is in the left most slot, then channel 2, the trigger module, channel 3 and channel 4.

V32 includes empirical correction into **@>ibias** and does monitor subtraction for **@>+ibias**, also changed I_BIAS_GAIN in cal0

V31 modified **@rpfn** to use right number of resistors.

V30 added line to !dcal to set legal data flag

V30 added phosphor trig enable to control register decoding when pulsed phosphor is selected

V29 added Itrip reset to **safe**

V29 is the earliest version shipped and was in unit 1.

V32 was the version shipped in unit 2.

An upgrade from V29 to V32 is available.

V29 will not operate in pulsed phosphor mode except through debug level commands.

11.2 INTRODUCTION

The hGXD software interface is similar to that of the GXD system.

The software in the control unit of the hGXD is reasonably simple and provides a comprehensive set of commands with a robust protocol. The hGXD is able to hide most of the details of the internal systems from the user.

11.3 TYPICAL OPERATION

The programme in the hGXD is stored in a serial EEPROM on the I^2C bus. On power up the programme is copied to RAM before execution. The limited bandwidth of the I^2C bus in this instrument gives rise to a delay of a couple of seconds or so after the application of power before the instrument will start executing the initialisation routines. After power up, the hGXD performs some initialisation of the head unit and reads which pulser modules are connected and where. From power up to being responsive takes about 41 seconds. After this the UCS can then proceed to send commands to set up the various voltages and enable supplies and enable triggering if appropriate. hGXD user configuration data is stored in volatile memory and it will be necessary to send commands to set up all the configuration data after power up or other reset events.

Note that each individual bias voltage can be set in the range -950 to +950, but the maximum voltage that should be applied between adjacent channels on the MCP may be much lower than this. It is the UCS responsibility to check that bias voltages are compatible, no check will be performed by the hGXDC.

There are status request commands that allow the UCS to check quickly that the hGXD is ready before a shot.

The various power supplies can be tested under supervision of the UCS by reading the monitoring ADCs. There is one temperature sensor fitted to the hGXD which should be monitored by the UCS and it is the users' responsibility to take appropriate action if overheating occurs.

11.4 ARCHITECTURE

hGXD consists of one control unit, one Comms. module, one trigger module and 4 pulser modules. The pulser modules generally have addresses 1 through 4 and these addresses correspond to the physical slots into which the pulsers are fitted, not to the particular pulser fitted. Delay data is pulser specific and the hGXDC reads which pulser is fitted where and uses the corresponding delay calibration. Currently the hGXDC only knows about pulsers supplied with the unit. A software upgrade in the future could make the hGXDC know about all pulsers manufactured. The production of such an upgrade will depend upon user feedback and requests.

11.5 HEALTH STATUS REGISTER

On power up the hGXDC tests the communication links to all modules 0 through 4. The **comms** bits of the health status register are initially set to zero, then each module found will have its corresponding bit set to 1. If a module is fitted to the hGXD and its **comms** bit is zero, this indicates a hardware problem.

The **comms 0** bit 8 is associated with the comms. module.

11.6 PFM MODULE CHECKS

The pulse widths are controlled by changing manually the PFN. Each PFM contains 3 resistors which are grounded at one end, the other end is pulled to ~2.4V by a 10k resistor in the PFN interface. The resulting voltages are converted to resistances by the hGXD and can be read using the **@PFN** command.

Each resistor can be one of ten different values which allows up to 1000 PFMs to be individually coded and remotely identified, which can be measured by the hGXDC and the values returned to the UCS.

It is important that the pulsers are enabled in order to check the PFM resistors, e.g. execute **30 !p%** before the **@PFN** command.

11.7 DELAYS

The delays are controlled by a relay switched delay line in each of the output modules 1 through 4, note this is not fitted to the special output module 1. To adjust the delays, the UCS must write the desired value for each module using the **!delay** command**.** The desired value can be read with **@delay.**

The delay circuit has 10 relays, which is slightly more than needed for 25ps resolution to 10ns. This is to allow manufacturing tolerances to be software trimmed using calibration data stored in the output module. Hence the pattern of relays for a given delay will vary from module to module and unit to unit. The hardware does not support direct absolute measurement of the relay pattern. However, if a read back is performed with the pulsers enabled, the hGXDC does a confidence check of the number of delay relays set against the expected value calculated from the delay setting. The result is obtained by reading the delay status with **@delaystatus**, The **delay OK** bits are set according to the test results. 1/0 indicates a pass/fail.

As the RF is turned off during a write cycle there is no need to prevent the unit from being triggered when changing the delays, the trigger module will not be powered and no signal will be propagating during a delay changing period.

11.8 ENABLE LOGIC

The enable logic of hGXD is different to GXD. In particular the hardware interlock on the front panel of the control unit will disable the RF power , the fast trigger circuit and the phosphor trigger circuit.

The reason for this is that disabling the RF power is the only fast way to turn things off, unfortunately it turns everything off. Consequently it is necessary that the trigger circuits are disabled so that the user is not misled into thinking that things are OK because the triggers are being detected.

It does not latch, the state of these three items and will toggle directly with the interlock state if they are enabled elsewhere. Figure 31 on page 39 shows the enable logic layout. The UCS may of course monitor the interlock status and issue a **safe** command if it is tripped.

11.9 PHOSPHOR

The phosphor supply is interlocked via the enable logic see Figure 31 on page 39. The desired value for DC or pulsed phosphor voltage can be set using **!vphosphor** and can be read back using **@ vphosphor**.

The hGXD is calibrated so that **!vphosphor** will give the correct voltage in DC mode if the phosphor return is connected. If the return is disconnected the output voltage will be higher due to the finite output impedance.

In pulsed mode, **!vphosphor** is not calibrated see .9.15 on page 28

The read back ADC monitors

i) the voltage on the phosphor return connection using **@>vrphosphor**

ii) the voltage on the phosphor high voltage power supply using **@>vpsphosphor**

In DC mode the voltages returned by **@>vpsphosphor** and **@>vrphosphor** should be a little different due to voltage drops on limiting resistors.

In pulsed mode only the **@>vpsphosphor** is useful.

The current from the phosphor power supply can be read with **@>iphosphor**.

The phosphor mode is selected as pulsed/DC by writing a 1/0 to the **pulsed phosphor** bit in the control status register. The phosphor trigger input can be selected as opto/electronic by writing a 1/0 to the **opto phosphor trig** bit. A phosphor trigger event sets the phosphor trigger latch, the state of which can be read as the **phosphor trigd?** bit and reset by writing a 1 to **reset phosphor trig latch**. This will not reset the gate trigger latch as in GXD. [Actually this may have been an error in the GXD manual as there are separate latches for gate and phosphor in GXD as well as hGXD].

There is no trip on the phosphor current.

The RF power is controlled by the hardware interlock so the phosphor power supply in the comms. module will power down if the interlock is not set in hardware. The interlock does not affect the enable status of the phosphor supply. This could be done by the UCS if needed. The interlock will disable the phosphor as it witches off the RF power but this is not a latched operation.

11.10 TRIGGER MODULE

The trigger module is enabled/disabled by writing a 1/0 to the control status register at bit 8 and its enable status can be checked at bit 8 after a read back, 1 = enabled, see section e) on page 47.

The RF power is controlled by the hardware interlock so the trigger module will power down if the interlock is not set in hardware. The interlock does not affect the enable status of the trigger module.

11.11 PULSERS

Each output module (i.e. each of modules 1, 2, 3 and 4) contains a high voltage pulse generator with power supply. The power supply is enabled/disabled by the hardware interlock. This is different from the GXD.

The pulser supplies can be **enabled/disabled** by writing 1/0 to the relevant **pulser enable** bits in the pulser status register using **!pulserstatus**, or read back using **@pulserstatus**. The current from the high voltage power supply can be read using **@ipulser**.

The RF power is controlled by the hardware interlock so the pulse modules will power down if the interlock is not set in hardware. The interlock does not affect the enable status of the pulser modules.

11.12 TEMPERATURE COMPENSATION

hGXD units have no temperature compensation. Bit 12 of the control register is used for forcing a write to the head.

11.13 LEDS

The GXD !leds and @leds commands have no effect in hGXD.

11.14 TEMPERATURE SENSORS

There is no over temperature shutdown built into the hGXD, it is the responsibility of the UCS to read the temperature sensor using **@temp** and take appropriate action. See section 9.16.1 on page 35 for location of the temperature sensor and normal working range readings.

11.15 PROTOCOL

The hGXDC will generate responses to valid commands and will not generate any unsolicited output. Invalid commands will be ignored. All commands and response will be in ASCII characters. Commands are case sensitive.

All commands will be parsed by the hGXDC using the Forth interpreter, so the parameters need to be delimited by spaces and the command line terminated by carriage return and linefeed characters. The Forth interpreter will not recognise any commands other than those defined in the command set.

The hGXDC will not echo command characters as they are received and no output will be generated until a valid command is recognised.

When a valid command is recognised, the hGXDC will output a response. Responses are preceded with a cr and lf, then an ascii **{** character and end with an ascii **}**. The response will be delimited into fields by an ascii **;** character. The first field in the response will be a repeat of the command. If the command cannot be completed the hGXDC will return an error code in the second field. The possible error codes are:-

?stack - the command interpreter has detected a wrong stack depth error, i.e. the wrong number of parameters have been received.

?param - the command interpreter has detected an out of range parameter.

After any error, the command is not executed, the stack is cleared and no values are returned other than the error code. Following a stack error, the stack is cleared then dummy parameters (generally -1 or 65536) are added for the purpose of formatting the response only.

All status commands expect and deliver data as decimal numbers and all numeric data should be decimal, no decimal points or other punctuation to be used.

For example:

1) to set the desired value of delay to 5000ps on channel 3, the command would be:-

5000 3 !d

and the response if the command can be completed would be:-

{5000 3 !d}

2) as above but with a missing parameter

3 !d

and the response would be:

{-1 -1 !d; ?stack}

The command interpreter detects the wrong stack depth, corrects this by clearing the stack and adding some dummy parameters then flags the error. No execution will result.

3) as above with invalid parameter

5000 9 !d

and the response would be:-

{5000 9 !d; ?param}

Again no execution will result.

4) to read the measure value of bias voltage on channel 2:

2 @>vb

and the response if the command can be completed would be:-

{2 @>vb; 100}

which implies the voltage is 100V

5) as above but with a missing parameter

@>vb

and the response would be

{-1 @>vb; ?stack}

6) as above but with an invalid parameter

9 @>vb

and the response would be

{9 @>vb; ?param}

11.16 THE STATUS REGISTER BIT DEFINITIONS

The hGXD is largely controlled by reading and writing to the status bits using the control commands. The status bits are as follows

a) Health status bits:

Bit	Description	R/W	Notes
b0	= not used		
b1	= not used		
b2	= not used		
b3	= not used		
b4	= not used		
b5	= not used		
b6	= not used		
b7	= not used		
b8	= comms 0	ro	1 = Comms. module found and ok, 0 = missing or fault
b9	= comms 1	ro	1 = pulser module 1 found and ok, 0 = missing or fault
b10	= comms 2	ro	1 = pulser module 2 found and ok, 0 = missing or fault
b11	= comms 3	ro	1 = pulser module 3 found and ok, 0 = missing or fault
b12	= comms 4	ro	1 = pulser module 4 found and ok, 0 = missing or fault
b13	= not used		
b14	= not used		
b15	= not used		

See section section 11.5 on page 41 for an explanation of bits 8 to 12.

b) Enable status bits:

Bit	Description	R/W	Notes
b0	= hw enable 0	ro	Read to find state of hw enable to module0
b1	= RF On/Off	ro	Bit is set if the RF power is logically ON. Note that if “disable RF on trigger” is set and the “fast gate triggered” is also set the RF power will be off. To restore RF power, either reset the fast trigger latch or disable the “disable on trigger” feature; both of these are in the control register, see section e) on page 47 Note that the RF power can be logically on but the power set to zero if nothing is enabled. The power level is set by what is enabled.
b2	= RF Tripped	ro	Use the “safe” command to reset the trip
b3 through b15 are unused			

c) Delay status bits:

BIT	Description	R/W	Notes
b0	= not used		
b1	= delay 1 ok	ro	1/0 = confidence test passed/failed for pulser slot 1
b2	= delay 2 ok	ro	1/0 = confidence test passed/failed for pulser slot 2
b3	= delay 3 ok	ro	1/0 = confidence test passed/failed for pulser slot 3
b4	= delay 4 ok	ro	1/0 = confidence test passed/failed for pulser slot 4
b5 through b15 are unused			

These bits are only valid if the pulsers were enabled during the last read back cycle. See section 11.7 on page 41 for an explanation of the function of the delay status bits.

d) Pulser status bits:

BIT	Description	R/W	Notes
b0	= not used		
b1	pulser enable 1	w r	Set=1 to enable =1 if enabled
b2	pulser enable 2	w r	Set=1 to enable =1 if enabled
b3	pulser enable 3	w r	Set=1 to enable =1 if enabled
b4	pulser enable 4	w r	Set=1 to enable =1 if enabled
b5 through 15 are unused			

See section 11.11 on page 43 for an explanation of the function of the pulser status bits.

e) Control status bits:

Bit	Description	R/W	Requires write cycle	Requires Read cycle	Notes
0	Phosphor soft enable	w r	Yes	 No	set=1 to enable =1 if software enabled
1	Phosphor enabled	ro		No	=1 if enabled
2	Pulsed Phosphor	w r	Yes	 No	set=1 to enable =1 if enabled.
3	Force Read Back	wo	No	Yes	set=1 to force immediate read
4	Phosphor trig opto	w r	No	 No	set=1 to enable =1 if enabled.
5	Phosphor triggered?	ro		No	=1 if triggered
6	Bias soft enable	w r	Yes	 No	set=1 to enable =1 if enabled.
7	Bias enabled	ro		No	=1 if enabled
8	HV trig enable	w r	Yes	 No	set=1 to enable =1 if enabled.
9	Fast trig enable	w r	No	 No	set=1 to enable =1 if enabled.
10	Reset phos. trig latch	wo	No		set=1 to reset
11	RF disable on trigger	wo	No		Set=1 to enable feature
12	Force write Read back valid	w r	Yes	 Yes	Set=1 to force immediate write =1 if read back valid
13	Fast gate trig opto	w r	No	 No	set=1 to enable =1 if enabled.
14	Fast gate triggered?	ro		No	=1 if triggered
15	reset fast trigger latch	wo	No		set=1 to reset fast trigger latch

11.17 CONTROL COMMANDS

Explanatory notes:-

1) In Forth terminology a @ character implies a fetch or read operation, a ! character implies a store or write operation.

2) % is used as an pseudonym for “status”.

11.17.1 BIAS VOLTAGE

Name	**!vbias**
Explanation	write desired value for bias voltage
Format	**x n !vb**
parameter 1	x = voltage, range -950 to 950 volts
parameter 2	n = channel number 1 through 4
returned value	none

Name	**@vbias**
Explanation	read desired value for bias voltage
Format	**n @vb**
parameter 1	n = channel number 1 through 4
parameter 2	none
returned value	desired value in volts

Name	**@>vbias**
Explanation	read measured value for bias voltage
Format	**n @>vb**
parameter 1	n = channel number 1 through 4
parameter 2	none
returned value	measured value in volts

Name	**@>ibias**
Explanation	read measured value for bias current
Format	**n @>ib**
parameter 1	n = channel number 1 through 4
parameter 2	none
returned value	measured value in μA/100, i.e. / 100 to get μA this measured value includes the current in the internal voltage monitor resistor.

Name	**@>+ibias**
Explanation	read measured value for bias current
Format	**n @>+ib**
parameter 1	n = channel number 1 through 4
parameter 2	none
returned value	measured value in uA/100, i.e. / 100 to get μA - this measured value excludes the current in the internal voltage monitor resistor.

11.17.2 DELAYS

Name	**!delay**
Explanation	write desired value for delay
Format	**x n !d**
parameter 1	x = delay, range 0 to 10,000 ps (rounded down internally to multiples of 25ps)
parameter 2	n = channel number 1 through 4 *Note change from GXD, there are now 4 channels.*
returned value	none

Note: channels have intrinsic delay of 0, 3ns, 6ns, 9ns for channels 1, 2, 3 and 4 respectively. This is not included in !delay.

Name	**@delay**
Explanation	read desired value for delay
Format	**n @d**
parameter 1	n = channel number 1 through 4 *Note change from GXD, there are now 4 channels.*
parameter 2	none
returned value	desired value in picoseconds

Note: Channels have intrinsic delay of 0, 3ns, 6ns, 9ns for channels 1, 2, 3 and 4 respectively. This is not included in @delay.

Name	**!fdelay**	*Not used in hGXD*
Explanation	write desired value for fine delay	
Format	**x n !fd**	

Name	**@fdelay**	*Not used in hGXD*
Explanation	read desired value for fine delay	
Format	**n @fd**	

Name	**@delaystatus**	
Explanation	read delay status - forces a confidence check of relay settings	
Format	**@d%**	
parameter 1	none	
parameter 2	none	
returned value	delay status	*Note 4 bits now used in hGXD*

Note: The delay status is only updated on a read back if the pulsers are enabled during the read back cycle. This is a hardware limitation that requires power to do the read back. If the pulsers are not enabled the delay status is not updated after a read back even if the delay settings have just been changed. This is obviously an area for future improvement. Feedback welcomed.

Name	**!gdelay**	*Not used in hGXD*
Explanation	write desired value for global delay.	
Format	**x !gd**	

Name	**@gdelay**	*Not used in hGXD*
Explanation	read desired value for global delay	
Format	**@gd**	

11.17.3 PULSERS

Name	**@pulserstatus**
Explanation	read pulser status
Format	**@p%**
parameter 1	none
parameter 2	none
returned value	pulser status

Name	**!pulserstatus**
Explanation	write pulser status
Format	**x !p%**
parameter 1	x = pulser status
parameter 2	none
returned value	none

Name	**@ipulser**
Explanation	read pulser supply current in HV supply circuit
Format	**n @ip**
parameter 1	n = channel number 1 through 4
parameter 2	none
returned value	pulser supply current in μA

Note: the hGXD hardware supports measuring the voltage also but we have not included this as it is not a GXD command. GXD hardware does not support measuring the voltage. Feedback welcomed.

11.17.4 LEDS

Name	**@leds**	*Not used in hGXD*
Explanation	read leds	
Format	**@l**	

Name	**!leds**	*Not used in hGXD*
Explanation	write leds	
Format	**x !l**	

11.17.5 PHOSPHOR

Name	**!vphosphor**	
Explanation	write desired value for phosphor voltage	
Format	**x !vph**	
parameter 1	x = voltage in volts range:-	
	0 to 3000 volts	*Range different from GXD. Pulsed voltage determined by load*
parameter 2	none	
returned value	none	

Name	**@vphosphor**
Explanation	read desired value for phosphor voltage
Format	**@vph**
parameter 1	none

parameter 2	none	
returned value	desired voltage in volts	
Name	**@>vphosphor**	*not used in hGXD*
Explanation	read measured value from phosphor output	
Format	**@>vph**	
Name	**@>vrphosphor**	
Explanation	read measured value from phosphor return	
Format	**@>vrph**	
parameter 1	none	
parameter 2	none	
returned value	measured voltage in volts	
Name	**@>vpsphosphor**	
Explanation	read measured value from phosphor power supply	
Format	**@>vpsp**	
parameter 1	none	
parameter 2	none	
returned value	measured voltage in volts	
Name	**@>iphosphor**	
Explanation	read measured value for phosphor current in high voltage circuit.	
Format	**@>iph**	
parameter 1	none	
parameter 2	none	
returned value	measured current, units μA	*Units change from GXD to hGXD*
Name	**!itrip**	*Not used in hGXD*
Explanation	write desired value for phosphor current trip	
Format	**x !it**	
parameter 1	x = current in arbitrary units, range 0 to 4095	
Name	**@itrip**	*Not used in hGXD*
Explanation	read desired value for phosphor current trip	
Format	**@it**	

11.17.6 PCD

Name	**!vpcd**	*Not used in hGXD*
Explanation	write desired value for pcd voltage	
Format	**x !vp**	
Name	**@vpcd**	*Not used in hGXD*
Explanation	read desired value for pcd voltage	
Format	**@vp**	
parameter 1	none	

parameter 2 none
returned value desired voltage in volts

Name **@>vpcd** *Not used in hGXD*

Explanation read measured value for pcd voltage

Format **@>vp**

parameter 1 none
parameter 2 none
returned value measured voltage in volts

Name **@>ipcd** *Not used in hGXD*

Explanation read measured value for pcd current

Format **@>ipc**

Name **@>+ipcd** *Not used in hGXD*

Explanation read measured value for pcd current

Format **@>+ipc**

11.17.7 PERSONALITY

Name **@version#**

Explanation read software version no.

Format **@v#**

parameter 1 none
parameter 2 none
returned value version no.

Note *unit 1 shipped with V29, unit 2 with V32; unit 1 should be updated to at least V32, see section 11.1 on page 40 for differences and section 12.1 on page 56 on how to upgrade the software.*

Name **@moduleid**

Explanation read module id

Format **x @mid**

parameter 1 x = module number, range 0 through 4
parameter 2 none
returned value module id

Note: *the trigger module in hGXD has no module id. This is a hardware limitation. Feedback welcome.*
For responses to this command see section 9.27 on page 37

Name **@rpfn**

Explanation read measure value of pfn resistor

Format **x n @rpf**

parameter 1 x =resistor number, range 1 through 3
parameter 2 n = channel number 1 through 4

returned value resistance in units of ten ohms
Note: The pulsers must be enabled to read back the PFN resistors, e.g. execute 30 !p%

Name **@controlserial#**

Explanation read control unit serial no.
Format **@cs#**
parameter 1 none
parameter 2 none
returned value serial no.
Note: The serial number returned is a simple number representing the unit number; section 9.26 on page 37 lists the serial numbers returned here against the real unit serial number.

11.17.8 MISCELLANEOUS MONITORING

Name **@temp**

Explanation read measured temperature

Format **x @t**

parameter 1 x = sensor number 0 through 16
parameter 2 none
returned value temperature in tenths of degree C
Note: there is only one thermistor in hGXD. All permitted values for parameter 1 return the same value.

Name **@itrigger**

Explanation read trigger HV supply current
Format **@itg**
parameter 1 none
parameter 2 none
returned value trigger supply current in microamps

Name **@vtrigger**

Explanation read trigger power supply voltage. *Change in what is read from GXD.*
Format **@vtg**
parameter 1 none
parameter 2 none
returned value trigger psu voltage in volts

Name **@isupply**

Explanation read RF current to the head. *Change from GXD*
Format **@>is**
parameter 1 none
parameter 2 none
returned value total supply current in mA

11.17.9 MISCELLANEOUS CONTROL

Name	**@healthstatus**
Explanation	read health status
Format	**@h%**
parameter 1	none
parameter 2	none
returned value	health status

Name	**@enablestatus**
Explanation	read enable status
Format	**@e%**
parameter 1	none
parameter 2	none
returned value	enable status

Note: The enable status has three active bits in hGXD, see section b) on page 45.

Name	**@controlstatus**
Explanation	read control status
Format	**@c%**
parameter 1	none
parameter 2	none
returned value	control status

Note: the control status register is considerably different in hGXD from GXD, see section e) on page 47.

Name	**!controlstatus**
Explanation	write control status
Format	**x !c%**
parameter 1	x = control status
parameter 2	none
returned value	none

Note: the control status register is considerably different in hGXD from GXD, see section e) on page 47.

Name	**safe**
Explanation	turns of RF power, disables everything, executes a write -read back cycle, restores the RF power.
Format	**safe**
parameter 1	none
parameter 2	none
returned value	none

*Note: **safe** is also used to reset the RF power if it has tripped, see section 9.19 on page 35*

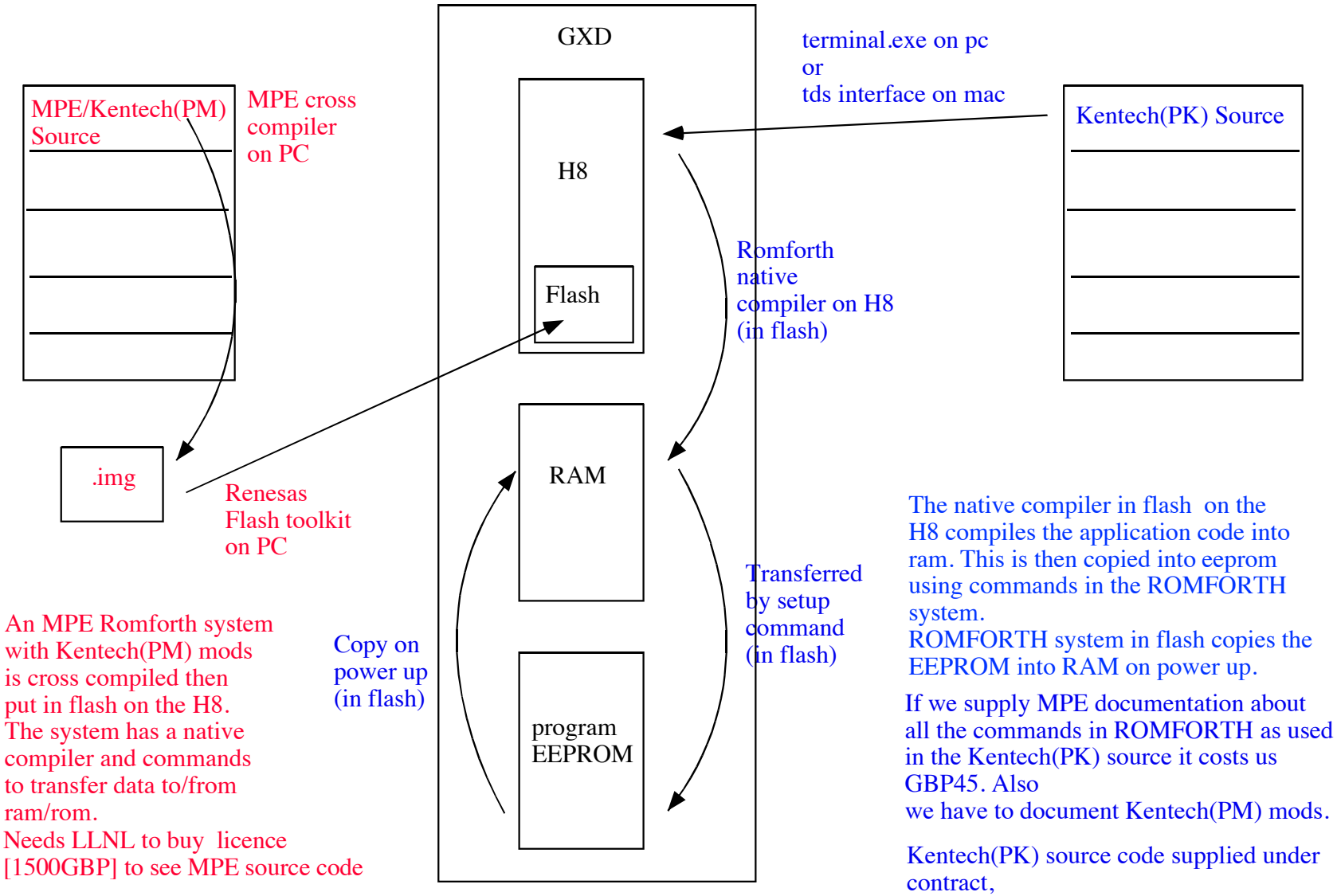


Figure 32 Software configuration

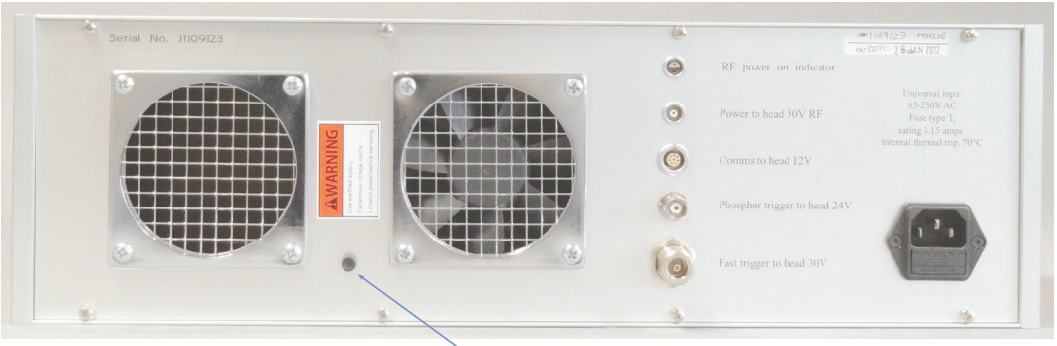


Figure 33 The location of the unmarked boot enable button on the rear panel

12 THE SOURCE CODE

The software inside the GXD is in two sections:-

The Forth operating system resides in the 128kbyte Flash memory of the Renesas H8S/2148F microprocessor.

The application programme resides in an I^2C serial EEPROM.

12.17.1 FORTH OPERATING SYSTEM

The Forth operating system uses MPE ROMFORTH. It was produced using the H8/330H and H8S Forth 6 Cross Compiler version 6.2 from:-

MicroProcessor Engineering Limited
133 Hill Lane
Southampton SO15 5AF
England

Tel: +44 (0)23 8063 1441
Fax: +44 (0)23 8033 9691
Skype: mpe_sfp
USA tel: (901) 313-4312

http://www.mpeforth.com/

Most of the source code for the Forth development system is proprietary to MPE and we are not allowed to disclose it unless the user purchases a licence for the Forth 6 Cross Compiler. It is not easy or meaningful to supply our modifications to the MPE code without also supplying sections of the original code. However it is possible to change the application programme without changing the Forth operating system so we consider that this is not strictly necessary and that it is beyond the scope of the current contract.

12.1 CHANGING THE APPLICATION CODE WITH A PC

12.1.1 WHAT IS NEEDED

You will need:

1 a PC running Hyperterminal or some other similar terminal emulator.

2 The PC should have a serial comms port or be fitted with a USB to RS232 adapter or Ethernet to RS232 adapter etc.

3 Access to both the front and rear of the control unit.

4 A suitable lead to go from the PC to the 9 pin DIN socket on the control unit of the hGXD.

5 A copy of the new code from Kentech Instruments.

12.1.2 CHANGING THE CODE

In the instructions below the phrase **(cr)** means type a carriage return.

1 Copy the new version file obtained from Kentech Instruments to your PC.

2 The following assumes you are using a PC with a simple serial coms1 port.

3 Connect the hGXD to the RS232 port of the PC and launch Hyperterminal.exe.

4 If Hyperterminal launches an existing connection just request a new one.

5 Name the connection, e.g. hGXD1

6 Select COM port 1 (assuming you have connected to COM port 1) and click OK.

Settings should be set to baud rate to 9600, 8 data bits, 1 stop bit and flow control to "none".

7 Select File/Properties

8 In the new pane select ASCII

9 In the new pane set the line delay to 25ms

10 Set the wrap text option to "yes". Hit apply/OK to close the pane and the next one.

11 Go to Transfer and set "Capture Text" to ON, set up a file called hGXD_log.txt

12 Switch on the hGXD controller, wait ~ 41 seconds for the system to become responsive.

13 Type **safe (cr)** the system should reply **{safe}**

14 Type **+debug (cr)** the system should reply **OK,**

15 You are now in debug mode and talking Forth to the device. Check this by typing **(cr)** a few times. The system should respond **ok** each time. Note that the state of the debug flag is stored in the calibration EEPROM, it is not affected by reset or power down. With the debug flag set the hGXD will always talk Forth on the RS232 rather than the normal protocol. In this state the normal protocol commands will still work but the received characters will also be echoed.

16 Press and hold down the Boot Enable button on the rear of the control unit. It is not marked but is shown in Figure 33 on page 56.

17 type **unsetup (cr)** the unit should respond with **ok-1**.

Release the boot flag enable button. The -1 in the response implies that there is one number on the Forth stack, this should be zero. Check this by typing a period "**.**" **(cr)** The unit should respond **0 ok .** If it returns a different number you have not erased the boot flag and possibly were not holding the boot flag enable button down firmly enough. Repeat the procedure, i.e. button down, type unset up etc. Alternatively there could be some other issue.

18 Turn off the power to the hGXD control unit for 5 seconds then turn it back on again. The unit should respond immediately with a header, possibly preceded with the message "No boot Flag".

You have now removed the old programme.

The programme setup flag is stored in the programme EEPROM with the application code. When powered up or reset, the hGXD reads the contents of this variable. If it is zero it drops into the Forth operating system, if it is non zero it reads the application programme from the EEPROM and executes it.

Check that communication with the unit is still OK by typing (**cr**) a few time and receiving (**ok**) each time.

Select Transfer/Send Text File from the menus. Browse to find the new software you have obtained and select it. This file will be sent to the hGXD. This process will take a few minutes.

Minimise the Hyperterminal window and open the log file (hGXD_log.txt) in an editor such as notepad++. Look for the character "^". You should not find any. If you have then the code has not downloaded to hGXD properly and you must repeat the procedure by cycling the power and downloading the file again, possibly with a longer pause at the end of each line (set up in properties).

If you find no "^" symbol in the log file go back to Hyperterminal and type

‘ inits (cr) the response should be **ok-1**

Note that there is a space between the ‘ symbol and inits. This command finds the location of the inits routine which is the first routine that hGXD has to execute on boot up.

Press and hold the boot flag enable button. Type **setup (cr)** and await the response **ok-1** after several seconds. The programme and boot flag have now been written to EEPROM. Release the boot flag enable button. Type a period "**.**" and you should see the response **0 ok**. This indicates that setup ran OK. Cycle the power (with a 5 second delay). The unit should become responsive after 41 seconds. The relays in the head should clatter during this period (if indeed the head is connected). After the 41 seconds the normal header should appear again. If the unit responds immediately after boot up then the boot flag has not been set and you will have to repeat the procedure.

You can type a few commands manually and check the responses as a confidence check if needed. You should at least try typing:

safe (cr)

When you are happy, reset the debug flag to leave debug mode by typing:-

-debug (cr) there is no response

The hGXD should now talk the normal protocol which can be checked manually, i.e. it will only respond to legal commands. Check the software version number by typing:

@v# (cr) the response should be **{@v#;32}** assuming you uploaded version 32.

12.2 CHANGING THE CALIBRATION

Unit 1 shipped with a poorly calibrated bias current monitor. Version 32 of the software has an improved calibration routine with some empirically found data but needs a different calibration number to be stored.

Set up communications with the unit as under section 12.1 on page 56 and enter debug mode by typing

+debug (cr)

The unit should respond **ok**

The variable that needs changing is called I_BIAS_GAIN. The underscores are part of the variable name.

type the following:

-1000 I_BIAS_GAIN ! the unit should respond **ok**

This stores the value -1000 in the variable I_BIAS_GAIN. The "**!**" is the store command. There is a space between -1000 and I_BIAS_GAIN and another space between GAIN and !

Next this needs to be stored in the EEPROM. Do this by typing:

ee!cal the response should be **ok** after a few seconds.

Cycle the power (5 second delay) and wait 41 seconds for the system to become responsive.

Check that the value of I_BIAS_GAIN is correct by typing:

I_BIAS_GAIN @ . (cr) the unit should respond **-1000 ok**

Note that there is a space between GAIN and @ and @ and . and . and (cr)

Put the unit back into normal command mode by typing:

-debug (cr) there should be no response.

Check the unit is ok by typing a legal command, e.g.

safe (cr) the response should be **{safe}**

Cycle the power (5 second delay) wait 41 seconds while the relays clatter in the head and then check the unit is responsive. You are now ready to go.

13 APPENDICES

13.1 CALIBRATION DATA

Table 4 Calibration data

Parameter	**hGXD1**	**hGXD2**	**hGXD3**	**hGXD4**
	J1007081	J1010221	J1109123	J1109124
	as shipped	as shipped	as shipped	as shipped
0 @moduleid	1	2	3	
1 @moduleid	11	1592	31	
2 @moduleid	12	2254	32	
3 @moduleid	13	1886	33	
4 @moduleid	14	1767	34	
@version#	29	32	34	
@controlserial#	1	2	3	
WRITE_DELAY	50	50	50	
READ_DELAY	50	50	50	
ADC_ZERO	2045	2045	0	
ADC_GAIN	-6124	-6124	-6112	
V_BIAS_GAIN0	1239	1020	1009	
V_BIAS_GAIN1	1022	1018	1025	
V_BIAS_GAIN2	1014	1025	1030	
V_BIAS_GAIN3	1019	1013	1030	
V_BIAS_ZERO0	-17	-36	-3	
V_BIAS_ZERO1	-65	-31	2	
V_BIAS_ZERO2	-65	-38	-3	
V_BIAS_ZERO3	-68	-37	-1	
I_BIAS_GAIN	200	-1000	-1000	
V_PULSE_GAIN	-1625	-1625	-1625	
I_PULSE_GAIN	256	256	256	
V_TRIG_GAIN	1625	1625	2000	
I_TRIG_GAIN	1613	1613	1613	
V_PH_RTN_GAIN	1014	1020	1020	
V_PH_RTN_GAIN	957	1020	1020	
V_PH_PSU_GAIN	1000	1000	1000	
I_PHOS_GAIN	-1000	-1000	-1000	
I_RF_GAIN	195	195	195	
SEND_TIMEOUT	10	10	10	
TH_T0	0	0	0	
TH_T1	25	25	25	
TH_T2	45	45	45	
TH_T3	80	80	80	
TH_T4	140	140	140	

TH_V0	4770	4770	4770	
TH_V1	2129	2129	2129	
TH_V2	1143	1143	1143	
TH_V3	508	508	508	
TH_V4	283	283	283	
RF_DP_B	0	0	0	
RF_DP_PH	3	3	3	
RF_DP_P	1	1	1	
RF_DP_B+PH	2	2	2	
RF_DP_B+P	1	1	1	
RF_DP_P+PH	1	1	1	
RF_DP_ALL	1	1	1	
RF_DP_NONE	1	1	1	
RF_PW_B	3	3	3	
RF_PW_PH	18	18	18	
RF_PW_P	19	19	19	
RF_PW_B+PH	15	15	15	
RF_PW_B+P	19	19	19	
RF_PW_P+PH	19	19	19	
RF_PW_ALL	19	19	19	
RF_PW_NONE	0	0	0	
REC_TIMEOUT	60	60	60	
R_MV_0	1284	1284	1284	
R_MV_1	1349	1349	1349	
R_MV_2	1416	1416	1416	
R_MV_3	1492	1492	1492	
R_MV_4	1578	1578	1578	
R_MV_5	1673	1673	1673	
R_MV_6	1781	1781	1781	
R_MV_7	1902	1902	1902	
R_MV_8	2037	2037	2037	
R_MV_9	2194	2194	2194	
R_MV_10	2371	2371	2371	
R_MV_11	2557	2557	2557	
R_MV_11	2557	2557	2557	

13.2 PFM RESISTOR CODES

The Pulse forming modules may be uniquely identified by reading the values of the three resistors in each module with the command **@rpf**. The resistor combinations are capable of distinguishing 9^3=729 modules. Table 5 shows the resistor values and labels for each module supplied under jobs

J1007081, J1010221, J1109123 and J1109124(a total of 2 units and 20 PFMs). Should the user need the codes of any modules supplied to other users please contact us. However, please note that modules are tailored to individual pulser channels and their performance when used on other pulsers even within an instrument have not been characterised. PFMs from hGXD will fit GXD units 1,2,7 and 8 but not 3,4,5,6 which were inadvertently fitted with inverted connectors to measure the PFM resistors. GXD PFMs will not fit hGXD as they are too wide.

Table 5 The PFM resistor codes and labels

PFM number	R1	R2	R3	Description
110	2.7	6.8	2.7	hGXD/PFM/J1007081/ch1/100ps
111	2.7	6.8	4.7	hGXD/PFM/J1007081/ch2/100ps
112	2.7	6.8	6.8	hGXD/PFM/J1007081/ch3/100ps
113	2.7	6.8	10	hGXD/PFM/J1007081/ch4/100ps
114	2.7	6.8	15	hGXD/PFM/J1007081/ch1/200ps
115	2.7	6.8	22	hGXD/PFM/J1007081/ch2/200ps
116	2.7	6.8	39	hGXD/PFM/J1007081/ch3/200ps
117	2.7	6.8	100	hGXD/PFM/J1007081/ch4/200ps
122	2.7	10	10	hGXD/PFM/J1010221/ch1/100ps
123	2.7	10	15	hGXD/PFM/J1010221/ch2/100ps
124	2.7	10	22	hGXD/PFM/J1010221/ch3/100ps
125	2.7	10	39	hGXD/PFM/J1010221/ch4/100ps
126	2.7	10	100	hGXD/PFM/J1010221/ch1/200ps
127	2.7	15	1	hGXD/PFM/J1010221/ch2/200ps
128	2.7	15	2.7	hGXD/PFM/J1010221/ch3/200ps
129	2.7	15	4.7	hGXD/PFM/J1010221/ch4/200ps
130	2.7	15	6.8	hGXD/PFM/J1010221/ch1/400ps
131	2.7	15	10	hGXD/PFM/J1010221/ch2/400ps
132	2.7	15	15	hGXD/PFM/J1010221/ch3/400ps
133	2.7	15	22	hGXD/PFM/J1010221/ch4/400ps
178	2.7	2.7	22	hGXD/PFM/J1109123/ch1/100ps
179	2.7	2.7	39	hGXD/PFM/J1109123/ch2/100ps
180	2.7	2.7	100	hGXD/PFM/J1109123/ch3/100ps
181	2.7	4.7	1	hGXD/PFM/J1109123/ch4/100ps
182	2.7	4.7	2.7	hGXD/PFM/J1109123/ch1/200ps
183	2.7	4.7	4.7	hGXD/PFM/J1109123/ch2/200ps
184	2.7	4.7	6.8	hGXD/PFM/J1109123/ch3/200ps
185	2.7	4.7	10	hGXD/PFM/J1109123/ch4/200ps
186	2.7	4.7	15	hGXD/PFM/J1109123/ch1/300ps

187	2.7	4.7	22	hGXD/PFM/J1109123/ch2/300ps
188	2.7	4.7	39	hGXD/PFM/J1109123/ch3/300ps
189	2.7	4.7	100	hGXD/PFM/J1109123/ch4/300ps
190	2.7	6.8	1	hGXD/PFM/J1109124/ch1/100ps
191	2.7	6.8	2.7	hGXD/PFM/J1109124/ch2/100ps
192	2.7	6.8	4.7	hGXD/PFM/J1109124/ch3/100ps
193	2.7	6.8	6.8	hGXD/PFM/J1109124/ch4/100ps
194	2.7	6.8	10	hGXD/PFM/J1109124/ch1/200ps
195	2.7	6.8	15	hGXD/PFM/J1109124/ch2/200ps
196	2.7	6.8	22	hGXD/PFM/J1109124/ch3/200ps
197	2.7	6.8	39	hGXD/PFM/J1109124/ch4/200ps
198	2.7	6.8	100	hGXD/PFM/J1109124/ch1/300ps
199	2.7	10	1	hGXD/PFM/J1109124/ch2/300ps
200	2.7	10	2.7	hGXD/PFM/J1109124/ch3/300ps
201	2.7	10	4.7	hGXD/PFM/J1109124/ch4/300ps