

# Kentech Instruments Ltd.

## Pockels Cell Driver



15th. December 1998

PLEASE READ THIS MANUAL CAREFULLY BEFORE USING THE PULSER

Unit 9, Hall Farm Workshops, South Moreton, Didcot, Oxon, OX11 9AG, U.K.

## Figure captions

Figure 1	The front panel	5
Figure 2	Conversion of TTL signal to Open collector drive for the HT enable signal.	6
Figure 3	Typical arrangement in Use	7
Figure 4	Output bias circuit	7
Figure 5	The trigger circuit	8
Figure 6	Power supplies	9
Figure 7	Logic	10
Figure 8	Trigger output stage	11
Figure 9	Trigger board layout	12
Figure 10	The stack	13
Figure 11	Reverse termination test results	15

### **DISCLAIMER**

This equipment contains high voltage power supplies. Although the current supply capacity is small, careless use could result in electric shock. It is assumed that this highly specialised equipment will only be used by qualified personnel.

The manufacturers and suppliers accept no responsibility for any electric shock or injury arising from use or misuse of this equipment. It is the responsibility of the user to exercise care and common sense with this highly versatile equipment.

## Contents

---

	<b>DISCLAIMER</b>	<b>2</b>
<b>1</b>	<b>INTRODUCTION</b>	<b>4</b>
1.1	SPECIFICATIONS	4
<b>2</b>	<b>GETTING TO KNOW THE INSTRUMENT</b>	<b>4</b>
2.1	FRONT PANEL CONTROLS, CONNECTIONS AND INDICATORS	4
2.1.1	CONTROLLING THE HT	5
2.1.2	THE VOLTAGE DISPLAY	5
2.2	REAR PANEL CONNECTIONS	6
<b>3</b>	<b>USE</b>	<b>6</b>
<b>4</b>	<b>CIRCUIT DESCRIPTIONS</b>	<b>7</b>
<b>5</b>	<b>TEST RESULTS</b>	<b>14</b>

## 1 INTRODUCTION

This manual describes the operation and use of the general purpose pockels cell driver.

### 1.1 SPECIFICATIONS

Voltage range	0.1 to 4.5kV as a switch up to reference voltage device.
Voltage reference	0 to -4.5kV.
Maximum repetition rate	Depends upon the load. For around 120pF it is 50Hz. For larger capacitors is set by the RC charging time of the load, $R \sim 10M\Omega$ .
Trigger input	3 volts 10ns f.w.h.m. into $50\Omega$ .
Jitter	Approximately 100ps or less (hard to measure)
Synchronisation Output	TTL approximately 30ns after trigger.
Main output	Switch to reference voltage approximately 33ns after trigger.
Remote HT enable	This input needs to be shorted to activate the HT. An open collector device rated at more than 12 volts will work. The turn on delay is about 100ms. The turn off delay is about 500ms for a 200pF load. The HT may also be enabled via a front panel switch.
TTL HT activate	This input requires a 5 volt $3\mu s$ pulse. Input impedance is 220k
Power input	Universal 85 to 264 volts A.C. at 47 to 440Hz. 2 amp fuse, type T (anti-surge) This unit contains an auto-resetting thermal trip rated at 70°C Maximum average power consumption 25watts.
Connectors	
Power	IEC
Trigger input	BNC
Synchronisation output	BNC
Output	SHV

## 2 GETTING TO KNOW THE INSTRUMENT

The pulser consists of a trigger circuit, some logic, a high voltage switch and an output bias section. The trigger circuit processes the incoming trigger signal, prevents multiple triggers and amplifies the signal to trigger the main switch stack.

The logic controls the voltage on the main switch and the DC bias voltage on the output. It also drives the panel indicators and controls the high voltage enable signals.

There are four LEDs which indicate the Power On, the HT On, ready and the trigger. Note that the unit can be triggered with the HT off. This is useful in setting up systems.

### 2.1 FRONT PANEL CONTROLS, CONNECTIONS AND INDICATORS

The front panel is shown in figure 1.

The backlight control turns on the backlight to the panel meter which indicates the voltage at the top of the switch.

Note also that the maximum repetition rate of 50Hz is only available for capacitive loads of around 120pF or less. More capacitive loads will take longer to charge and hence limit the repetition rate. In practice the unit may be triggered at up to 100Hz, independent of the load but the load capacitor may not have had time to recharge and so will not be at the voltage indicated by the panel meter. No damage will be done to the unit by switching capacitors up to around 1nF. However, the stack is only turned on for about 80ns, so the load capacitor must be significantly smaller than 1.0nF for the voltage to be pulled down to ground.

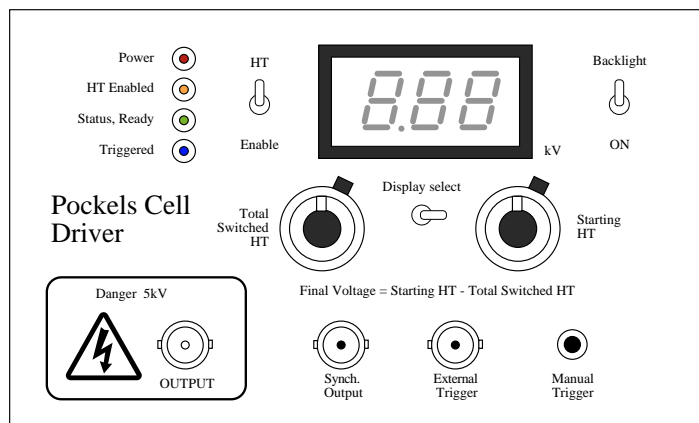


Figure 1 The front panel

### 2.1.1 CONTROLLING THE HT

The HT may be controlled with any of three systems. The HT enable systems turn on the voltage to the high voltage switch and the to the bias circuitry. However, these systems are independent, i.e. their “ON” states are ORed together. This means that the HT is off only if all three systems are holding it off. In general the operator is expected to use one system to manipulate the HT and the other two will be in an off state.

The three systems are:-

- 1 Front panel HT enable momentary action switch
- 2 Rear panel HT enable input, short to enable.
- 3 Rear panel latched HT enable with auto disable on trigger.

The front panel HT enable switch. It is a momentary action switch. The unit will always power up with the HT off unless one of the other two systems is active.

The rear panel HT enable circuit. Allow around 100ms for the power supply to charge up the output stage. The State of the HT follows the state of this input. i.e. short to enable, open circuit to disable. This can be driven with a relay or with an open collector transistor rated at 12 volts.

The rear panel latched HT enable is designed so that the HT is applied to the load only until a trigger is received. This allows the enabling circuit to be decoupled from the firing circuit. On receipt of a signal (5 volts for 3 $\mu$ s) the HTs will enable. The trigger circuit will disable the HTs. Note that if it is necessary to disable the HTs manually the manual trigger button should be pressed. THE HT disable switch will not switch the HTs off. (It is likely that this will changed on future units)

The delay in bringing the HTs up to voltage depends upon the actual settings. At the output of the unit is a 4.4nF capacitor. One side is set to the total switched HT and the other side (the output) is set to the starting voltage. If these are set to the same value then the capacitor does not have to be charged before the shot and so the time taken to charge up the system is reduced. However, to be sure that the voltages have reached the stable state one should allow 100ms.

On receipt of a trigger pulse the HTs are disabled. One should allow 100ms for this to decay to zero.

### 2.1.2 THE VOLTAGE DISPLAY

The voltage displayed on the panel meter can be switched between the bias voltage, i.e. the output starting voltage and the switch voltage, i.e. the total switched HT.

The final voltage is the difference between these two settings.

The panel meters actually display the reference voltage that is used in the voltage stabilisation circuit, not the actual HT. When the HT has reached the required level the blue Ready light is illuminated and the ready output on the rear panel goes to 5 volts (TTL high).

If the output is loaded resistively it may be that the supply cannot raise the HT sufficiently and in this case the ready light will remain out. Similarly if the switch fails in some way and cannot take the voltage the ready light will not come on. One can find out which is at fault by turning down the HT on each separately and seeing if this causes the ready light to come on.

The triggering circuit will operate even when the HT is off or on but not ready. The panel meter will only indicate the charge voltage when the HT is on and the ready light is illuminated.

The HT voltages are set with a multiturn potentiometers. Their positions may be locked. Allow the unit to warm up for several minutes before setting a voltage as the feedback resistive divider chain uses resistors that are not well thermally coupled.

There are three front panel connectors. The trigger input, the synchronisation output and the main output. It is the main output that is switched on receipt of a trigger signal.

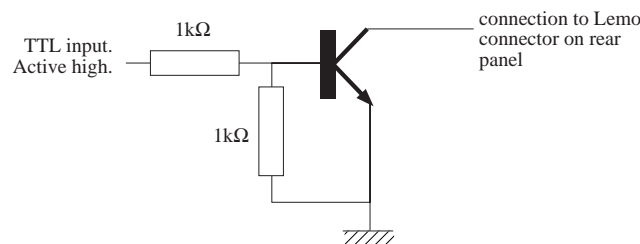


Figure 2 Conversion of TTL signal to Open collector drive for the HT enable signal.

## 2.2 REAR PANEL CONNECTIONS

There are four rear panel connections: the power inlet with switch and fuse, the remote HT enable, the remote HT activate with latch and the ready output. The power inlet is filtered and will accept IEC leads. It uses a universal supply that will run from a variety of AC voltages, see specification.

The HT enable (Lemo size 00) socket requires to be short circuited to enable the HT supply. An open collector device with voltage rating in excess of 12 volts and minimal current capability can be used. If a pulse response is required it will be necessary fit a single transistor stage in open collector configuration across this input, see figure 2

The HT activate (Lemo size 00) requires approximately a 3µs 5 volt pulse into 47kΩ.

The ready output (BNC) is a 5 volt from 10kΩ (TTL) output.

## 3 USE

The pulser may be used in a variety of ways depending upon the application. The unit is basically a high voltage switch to a reference voltage through a 50Ω load resistor. Figure 3 indicates the normal operating arrangement.

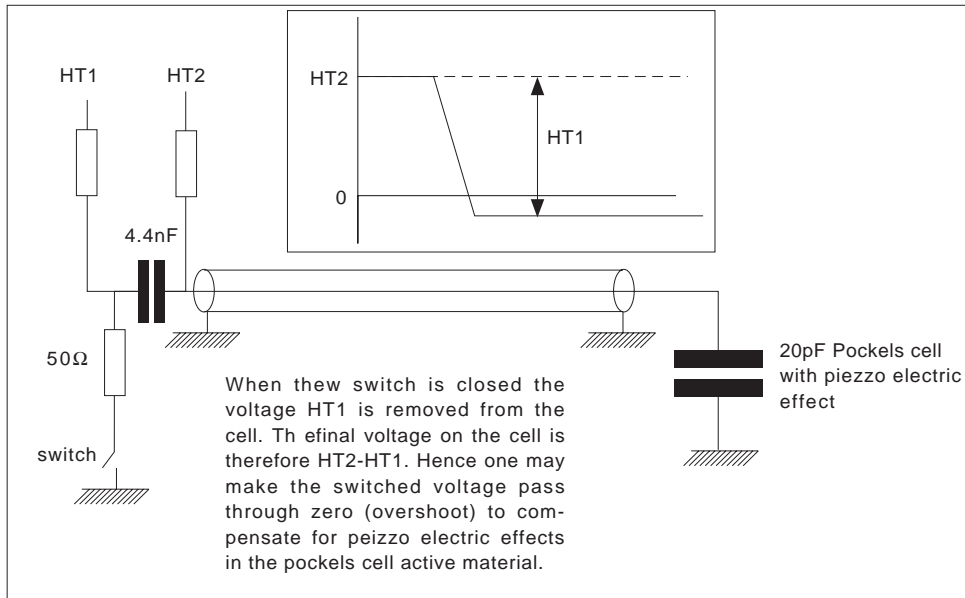


Figure 3 Typical arrangement in Use

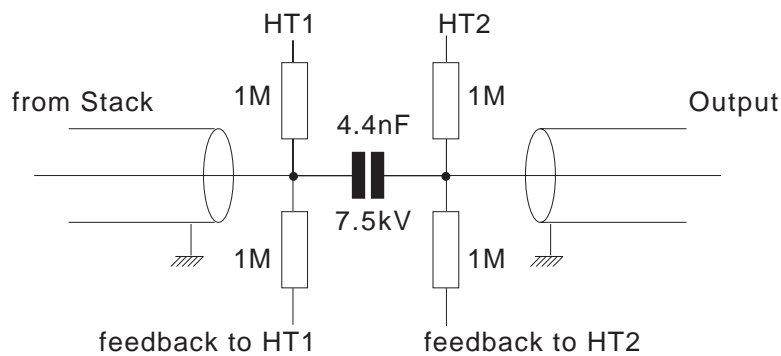


Figure 4 Output bias circuit

#### 4 CIRCUIT DESCRIPTIONS

The circuit consists of a high voltage series parallel array of 1kV FETs 72 arranged 12 wide and six high. This is driven by a single trigger pulse that is transformer coupled to all the fets. The switch switches to ground but there is a  $46\Omega$  resistor connected between the high voltage side of the stack and the output. The output is also connected to the HT supply via a  $1M\Omega$  resistor. The HT is monitored via a second  $1M\Omega$  resistor and this signal is used to stabilise the voltage.

The stack is protected against breakdown and over voltaging with zener diode chains. A resistive chain down the stack also allows the unit to run at lower voltages whilst maintaining the equal distribution of voltage across each stage.

The trigger circuit delivers around 650 volts into  $25\Omega$  and is also a FET pulser with four similar FETs to those used in the stack.

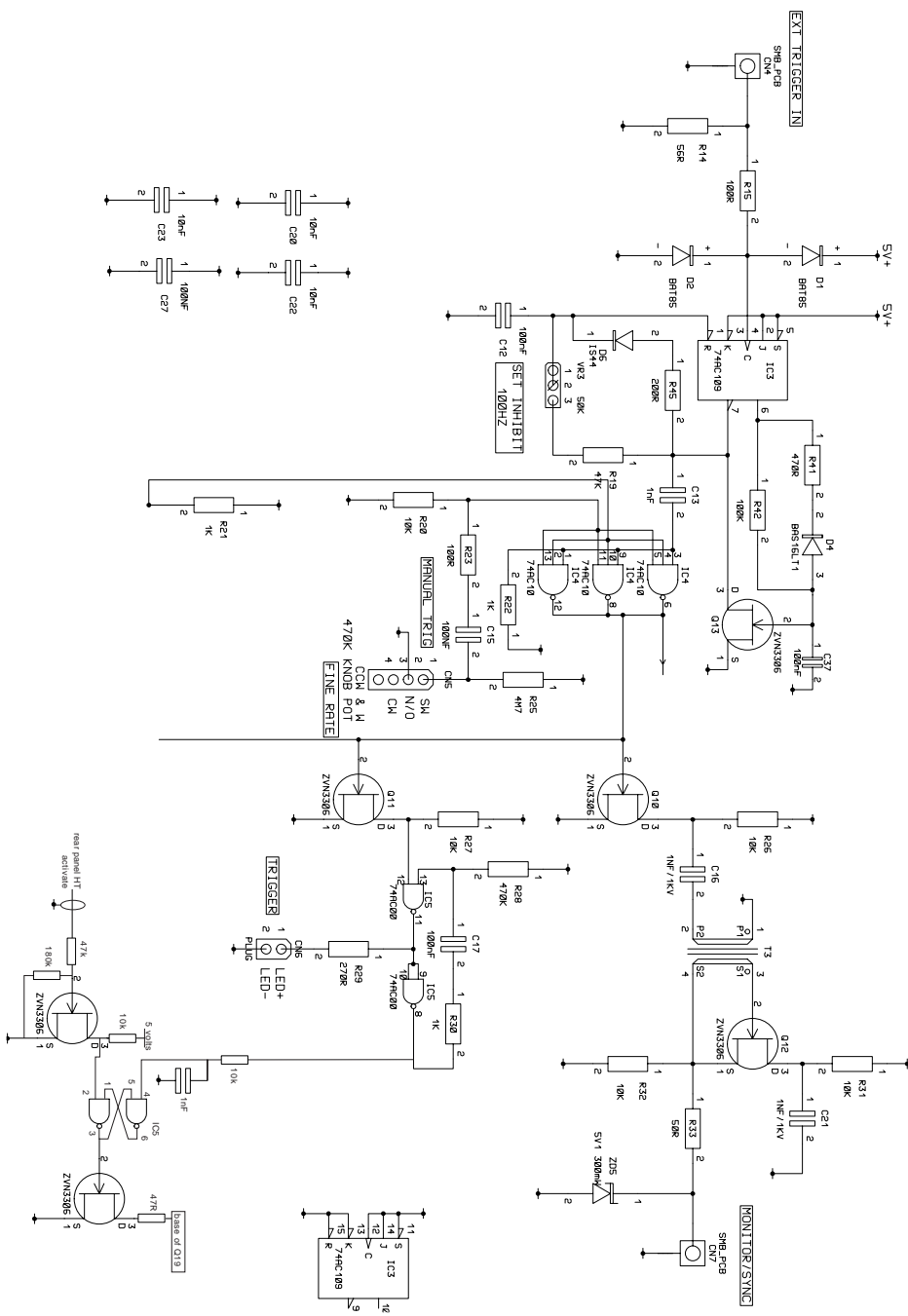


Figure 5 The trigger circuit



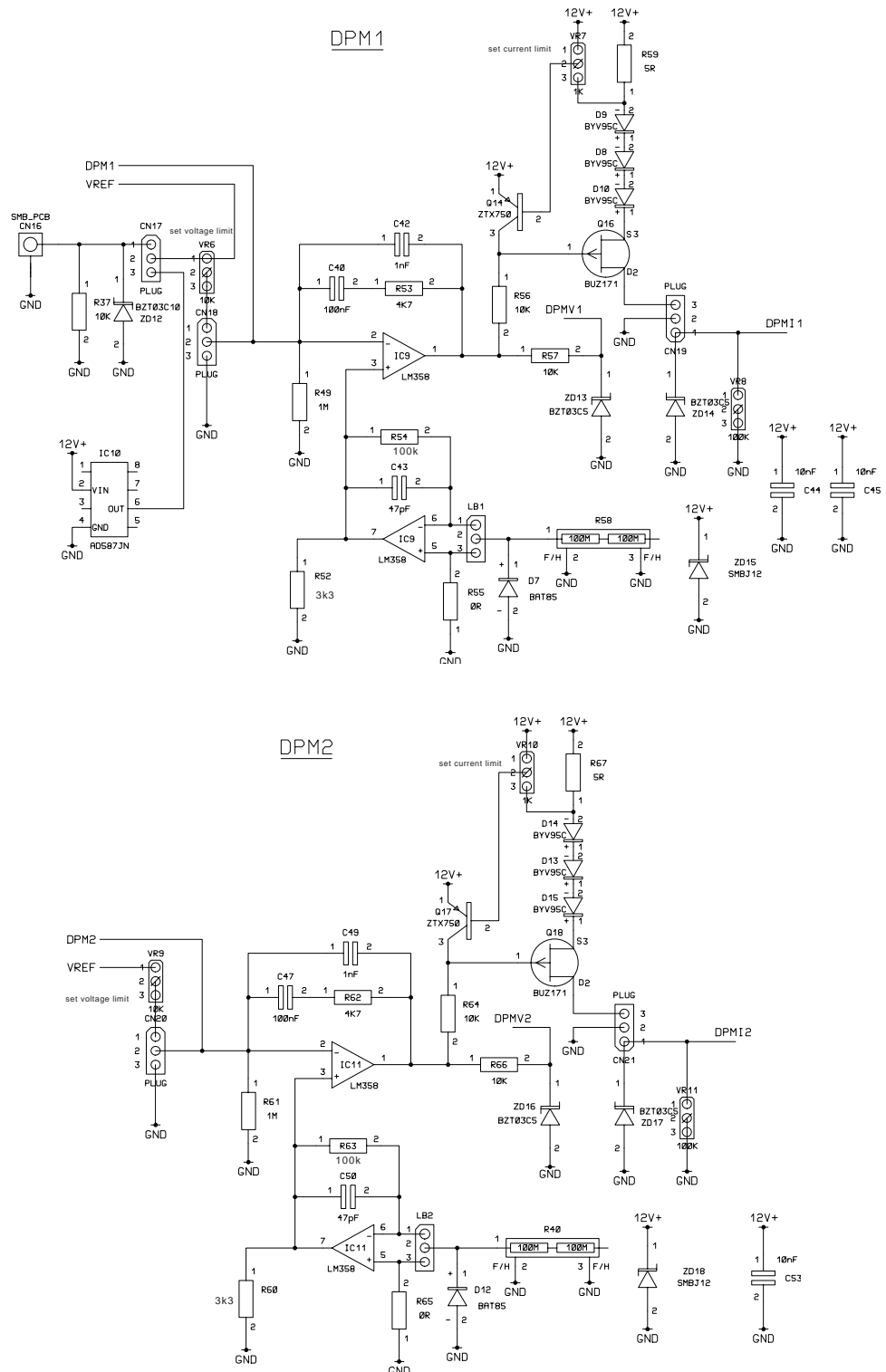


Figure 6 Power supplies

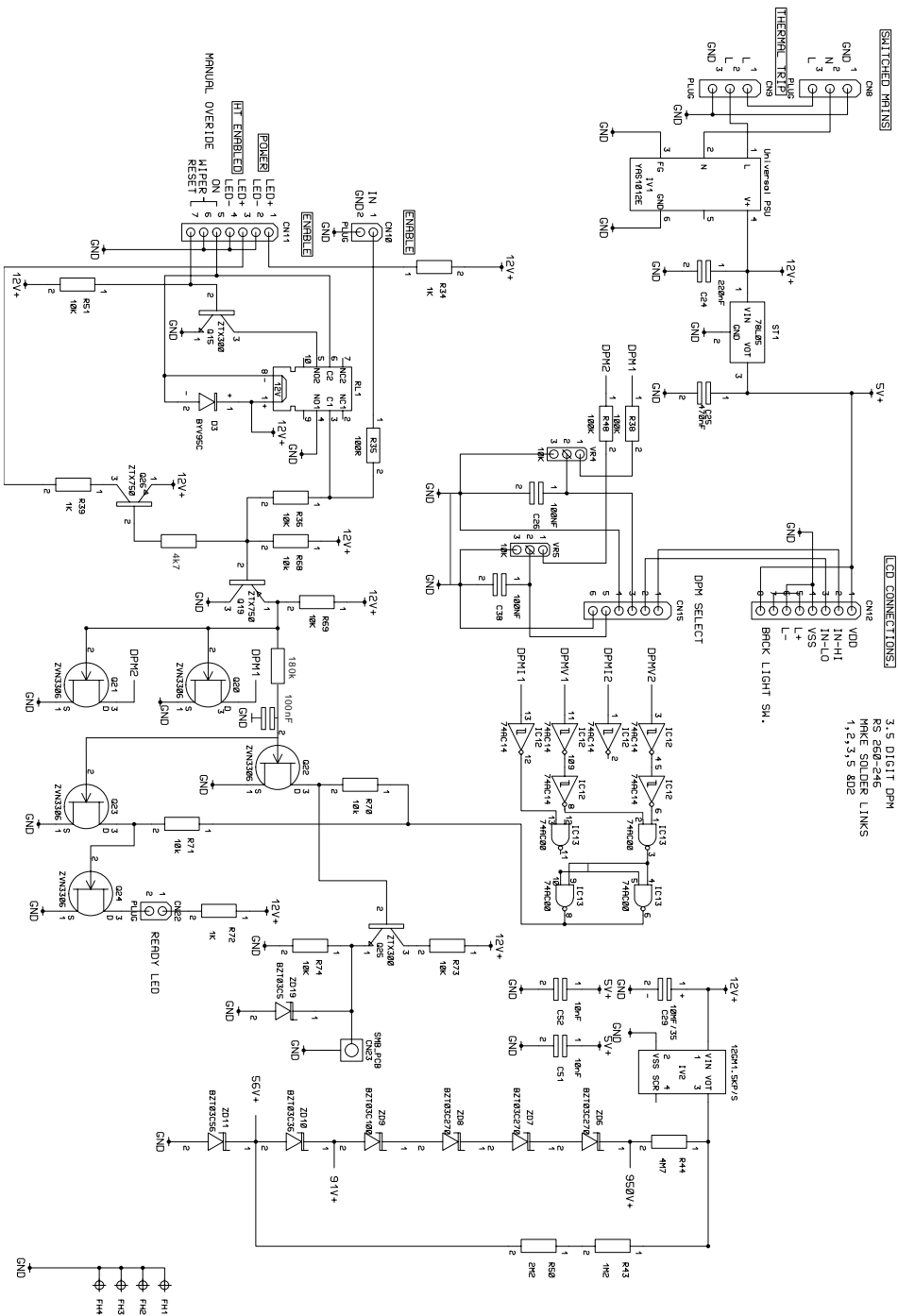


Figure 7 Logic

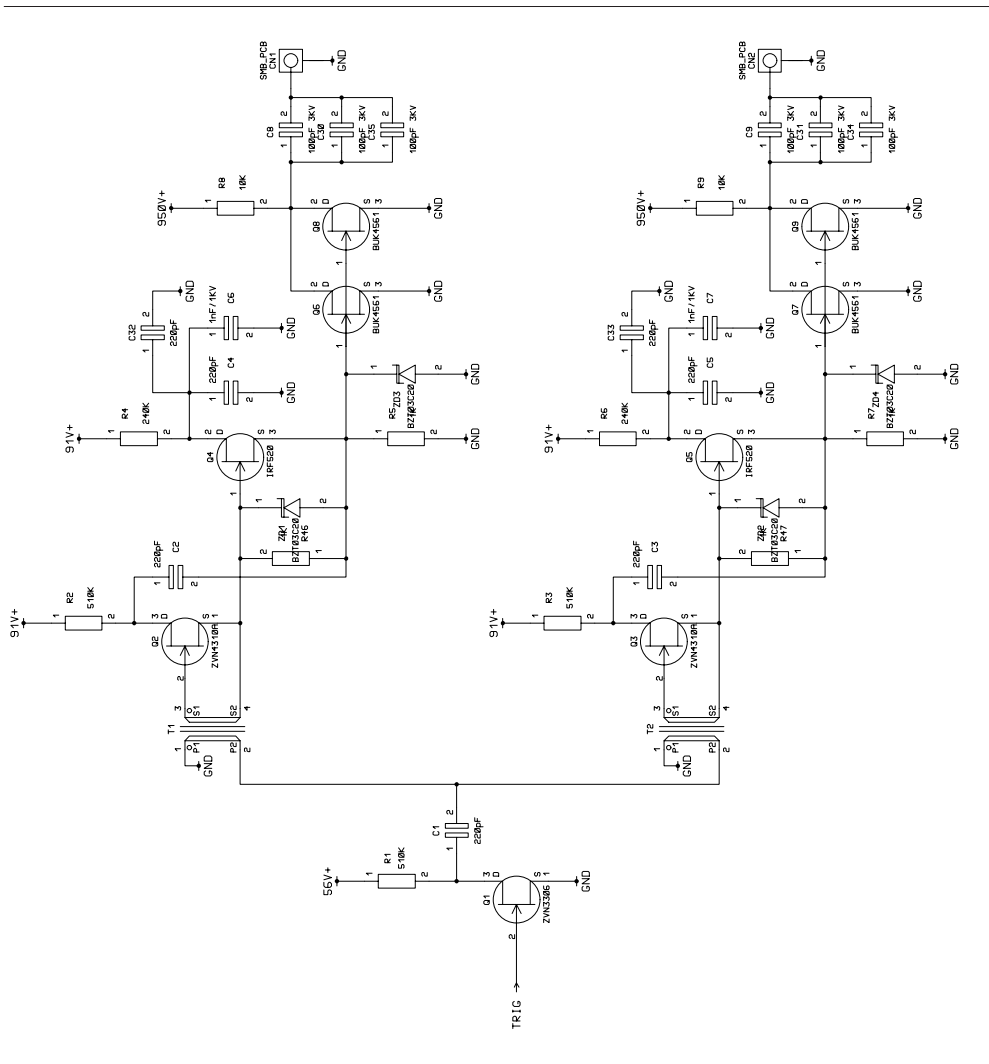


Figure 8 Trigger output stage

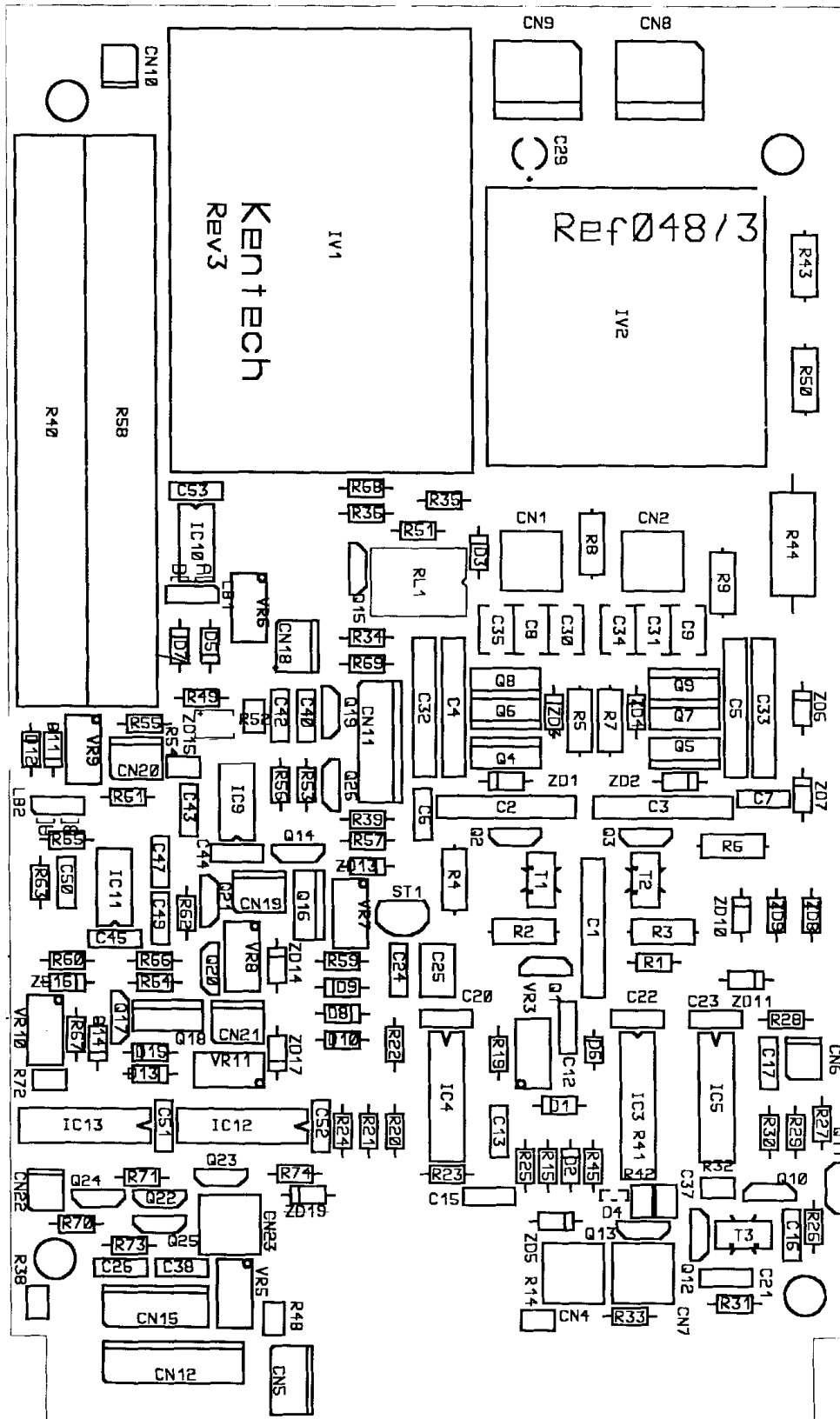


Figure 9 Trigger board layout

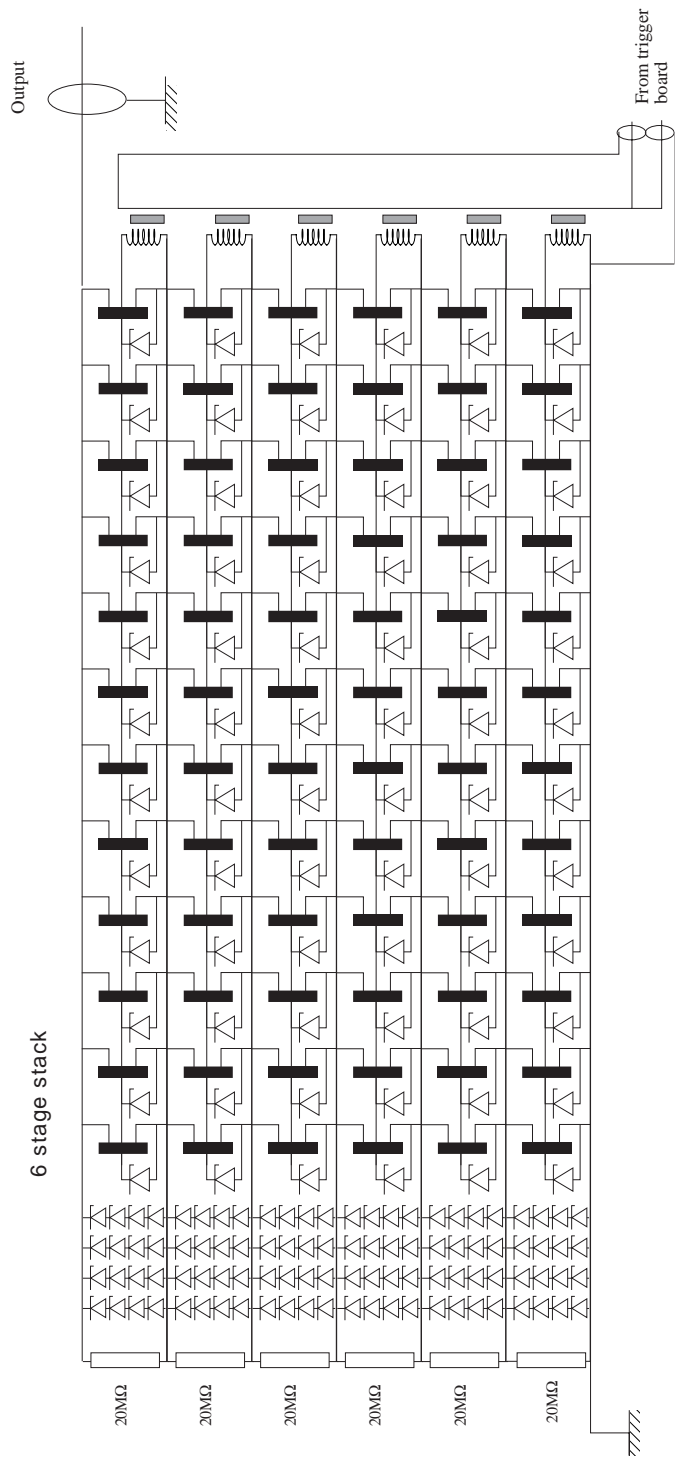


Figure 10 The stack

## 5 TEST RESULTS

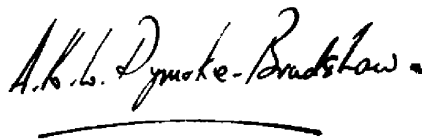
The following tests have been done and setup procedures followed:-

- 1 Set up upper voltage limit of HT1 to less than zenner voltage on stack. Typically set to just over 4.5kV.
- 2 Set up upper voltage limit of HT2 to the same as HT1.
- 3 Set up digital meter calibration on both HT1 and HT2, check calibration over full voltage range, (typically within 3%)
- 4 Using the monitor output, set up repetition rate limit to around 100Hz.
- 5 Check that the remote HT enable operates correctly.
- 6 Check that the remote HT activate operates correctly.
- 7 Check that the switch operates reasonably into a Tektronix high voltage probe (P6015 used).

Results as follows:-

- (a) with no trigger the signal should be DC at HT2 set on the front panel (Start voltage.
  - (b) With a trigger the voltage should fall to start voltage - switch voltage approximately 40ns after the trigger. The fall time will be around 5ns and will probably be limited by the test gear.
- 8 Check that the reverse termination of the pulser is correct. This is done in the following manner:-
- (a) Connect the main output to a  $50\Omega$  cable of at least 8ns transit time. Connect this to a second cable of around 1ns transit time with a 22pF capacitor in series with the inner conductor. It is important to maintain a low inductance path around the capacitor and yet to ensure that it will hold off 5kV.
  - (b) The output of the second cable goes into 60dB of attenuation into an oscilloscope with a bandwidth of several GHz, typically a sampling oscilloscope.
  - (c) The oscilloscope should display a single spike representing the differential of the edge arriving at the capacitor. At around 20ns later there may be a residual spike, of either polarity, representing the reflection of the edge from both the capacitor and back from the pulser. If the pulser reverse termination is perfect there should be no second spike. In practice the reverse termination is (a) not perfect and (b) voltage dependent as the resistors used are not perfectly linear with voltage. If the spike is significant, calculate the reflection coefficient at the pulser, from this derive the effective reverse termination resistance. Compare this to that fitted and adjust as necessary. This will entail partial dismantling of the main switch assembly and should only be done at the factory.

All tests Passed.



A. L. Dymoke-Bradshaw

Reflection test with 20pF capacitor  
terminating resistors are 14 x 68  $\Omega$  resistors  
arrange to give 46.36 $\Omega$  terminating resistance.  
This is at maximum HT and indicates the worst case reflection.

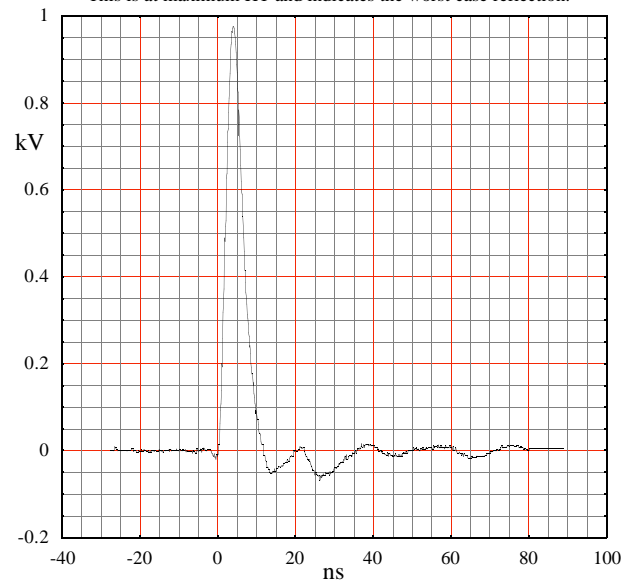


Figure 11 Reverse termination test results