# Kentech Instruments Ltd.

# Instruction Manual
# for
# SIMCART pulse generator system

Serial Numbers J99*****/1 and J99*****/2

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PLEASE READ THIS MANUAL CAREFULLY

BEFORE USING THE PULSE GENERATOR

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# Figure Caption

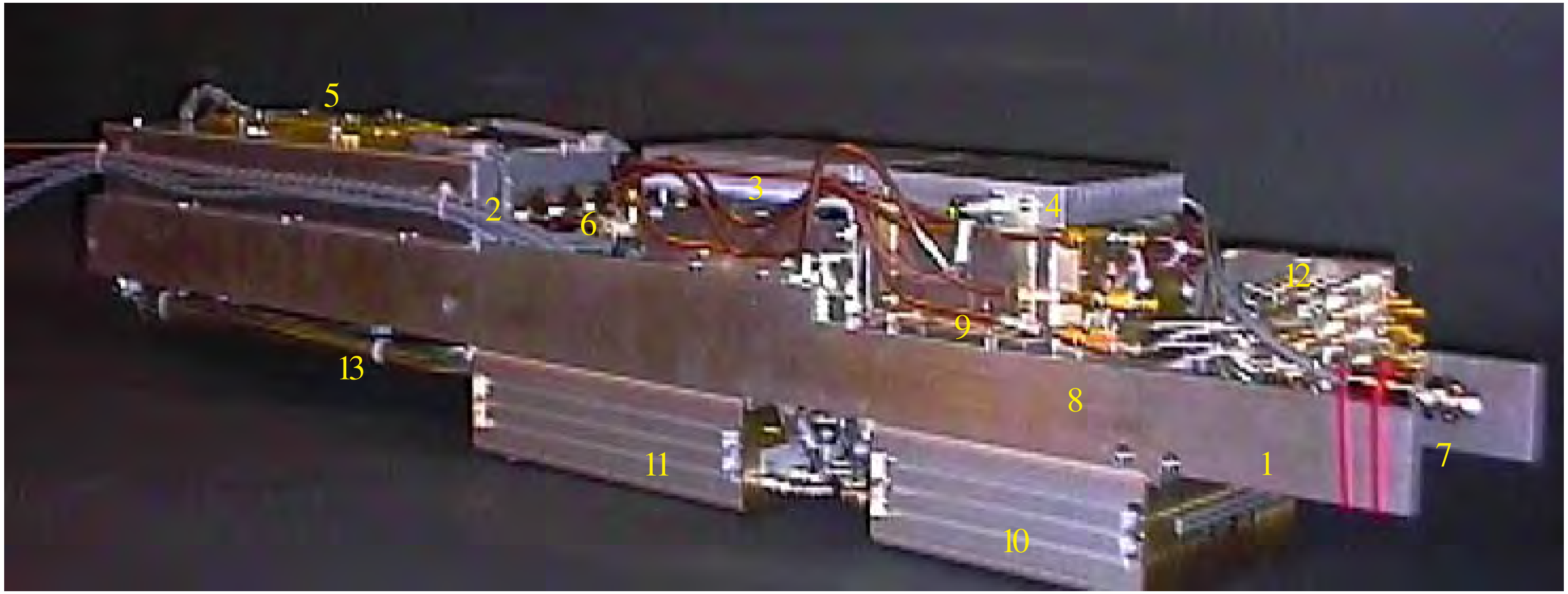



Figure 1 The system

1 Mounting frame
2 Four channel pulse generator
3 Four channel delay unit
4 Six rail power supply
5 Sliding trombones for timing set up
6 Pulse forming modules
7 HT connection to phosphor
8 DC blocks
9 Output cables
10 Computer and power supply regulators
11 Auxiliary power supply and high voltage monitor box
12 Bias insertion, terminator and pulse monitoring box
13 Delay cables for pulse monitoring

# 1 INTRODUCTION

This manual describes the use of a fast gated x-ray Imager. Originally it was designed for use in SIMTUBES on the Nova Laser at LLNL. Since then it has undergone several stages of evolution. The units supplied here are not designed with a specific chamber in mind.

The unit will eventually consist of a gated microchannel plate x-ray detector, phosphor with film or CCD readout and an electronics package to drive and monitor it. Supplied with this manual is just the electronics package to drive the head. No readout electronics, head or photoconductive detector (PCD) is included.

This manual describes a complete system although Kentech Instruments Ltd. is only supplying the electronics control package. Some descriptions may not be relevant to other parts of the system, depending upon how it is assembled and the type of detector head used.

The whole package was originally designed to fit on a cart that will go through a six inch tube as used on laser target experiments. However, the tubes on current facilities are larger and so the six inch limit has not been adhered to. In addition no cart is supplied here, just an assembly to hold the parts together.

The system is designed to work under vacuum and the design has allowed as much as is feasible for the cooling of electronics by thermally coupling them to the structure and also trying to avoid trapped volumes and poor vacuum materials. However, the nature of electronics means that the surface area will be large and pump down times will be significant for a unit that has been at atmospheric pressure for a long time and also handled etc. We have tested that these units pump down to around $3.\ 10^{5}$ torr in around 15 minutes in our small test facility.

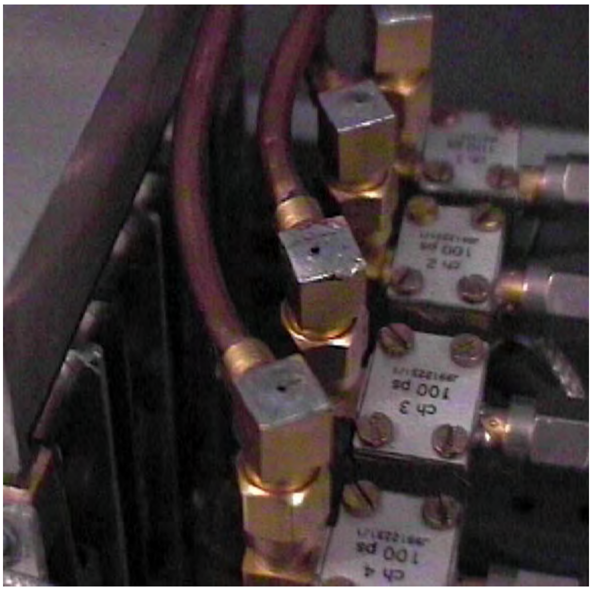


Figure 2 Vented connectors

## 1.1 LAYOUT AND PRINCIPLES OF OPERATION

A complete system comprises a detection head with film back (or other image recording system), and an electronics package to drive it. The electronics contains DC power supplies, gating and delaying electronics and monitoring circuitry.

The detection head consists of a specially coated MCP with fast connections, a phosphor screen and a film pack. The electronics is connected to this. On the electrical input side there are the pulse forming circuits. On the output side the bias voltages to the MCP strips are inserted, the pulses are absorbed in the terminator and there is the pulse monitoring circuitry. Added to this is a bias insertion, terminator and monitor for a signal from a PCD. This signal is added in to the pulse monitors to give the relative timing of when the source signal reaches the detector.

Specification

| | |
|---|---|
| typical gate lengths | 100ps (with suitable heads) and 1ns |
| Electrical specification | see section 2.1 about the power supply. |
| Typical detector | ø40mm, 4 x 12Ω strips on Galileo MCP. L/D = 40 |
| Typical PCD | Diamond 1 x 1 x 1 $mm^3$ |
| Delays | Any channel 0 to 12.7ns in 100ps steps* |
| Gate pulses | The gate pulses from the pulser are 2.5 to 3.5kV depending upon gate length, see pulse shapes at the rear of the manual. |
| Monitor | Pulses are resistively combined with successive 15 ns relative delay along with the PCD monitor signal and fed to the SIMCART output coaxial connector. |

* These delays are nominal. Difficulty in manufacture and variability in cable velocity of propagation mean that delays will not be as indicated. However the delay is monotonic with setting. The calibration of the delays for unit J9912231/1 is shown in figure 27.

## 1.2 FAST GATING METHOD

The X–rays which are incident on the MCP produce photoelectrons. With a voltage across the MCP some of these will be accelerated into the MCP and generally hit the sides of the holes in the plate where they will multiply as they cascade down through the MCP. At the output they are then accelerated onto the phosphor screen producing light which may be recorded with an integrating detector. Gating is achieved by changing the voltage across the MCP very quickly. To do this the MCP is coated with a gold on copper strip to form a transmission line between the top (input) and bottom (output). The glass of the MCP forms the dielectric of the transmission line and determines the speed of propagation of the gate pulse across the face of the MCP. The dielectric constant of the MCP material is high, although this is reduced to a lower effective value by the holes. The result is a low velocity and a transmission line of low impedance. The combination of high gate voltage and low impedance means that the currents involved are considerable, making connections to the MCP particularly difficult. The gate drive electronics has to drive this impedance which will be only a few ohms for useful gated areas.

## 1.3 CARE AND ENVIRONMENTAL CONSIDERATIONS

**PLEASE READ THIS SECTION CAREFULLY**

The microchannel plate is an array of about $12.5 .10^6$ single channel electron multipliers fused into a precision matrix. It is fabricated from a lead doped glass and the performance can be affected greatly by adverse environmental conditions or other maltreatment.

The lining to the walls is about 1µm thick and is easily damaged. Consequently proper handling precautions must be observed to retain the performance.

No object should come into contact with the sensitive area of the MCP. When handled the MCP should be held only by the border. All tools and other implements that touch this area should be clean and degreased and made of materials compatible with a high vacuum environment

The heads or MCP containers should only be opened under class 100 laminar flow clean room conditions. Should any particles become affixed to the plate they should be removed using a single hair brush and an ionised dry nitrogen gun.

The MCP is hygroscopic and must be stored correctly. Ideally this means an oil free vacuum. Alternatively they may be stored in a dry inert gas. Desiccators using silica gel have proven **unacceptable.**

Some MCPs, particularly those with a hard edge, can bow if they absorb moisture. Should this happen the head may well not work properly due to the uneven spacing between the phosphor and the MCP and may even break down. Bowing may be corrected by heating the MCP in a vacuum oven at 300° C for 3 hours or until flat.

The phosphor screen is also a very delicate part of the head and should be treated with care. Nothing should be allowed to come in contact with the aluminium layer. Particulate contamination of the surface is best removed with an ionised dry nitrogen gun.

### 1.4 GENERAL ELECTRICAL LAYOUT

The electronics consists of several modules, namely:-

- Pulse generator
- pulse forming modules
- delay unit
- main power supply
- Auxiliary power supply and voltage monitors
- Computer interface
- Bias insertion and pulse monitoring and combining circuitry.

A schematic of the circuit is shown in figure 3.

## 2 THE ELECTRONICS

The pulse generator is a four channel system with independent delay control of each channel. The power supplies offer outputs to bias a gated microchannel plate detector system.

The overall specification is as follows:-

### 2.1 POWER SUPPLY SECTIONS.

There are nine high voltage power supply rails indicated and specified as follows:-

Input voltage 12 volts DC ±15%

Input current 1.8 amps average

1 Phosphor voltage 0 to 6kV in 750 volt steps at 20µA

2 Spare 0 to 1kV in 50 volt steps at 100µA

3a Bias voltage for channel 1 -1kV to +1kV in 50 volt steps at 100µA

3b Bias voltage for channel 2 -1kV to +1kV in 50 volt steps at 100µA

3c Bias voltage for channel 3 -1kV to +1kV in 50 volt steps at 100µA

3d Bias voltage for channel 4 -1kV to +1kV in 50 volt steps at 100µA

4 Bias voltage for PCD 0 to 1kV in 100 volt steps at 20µA

5 -4kV for pulser at 2mA

6 -3kV for pulser at 1mA

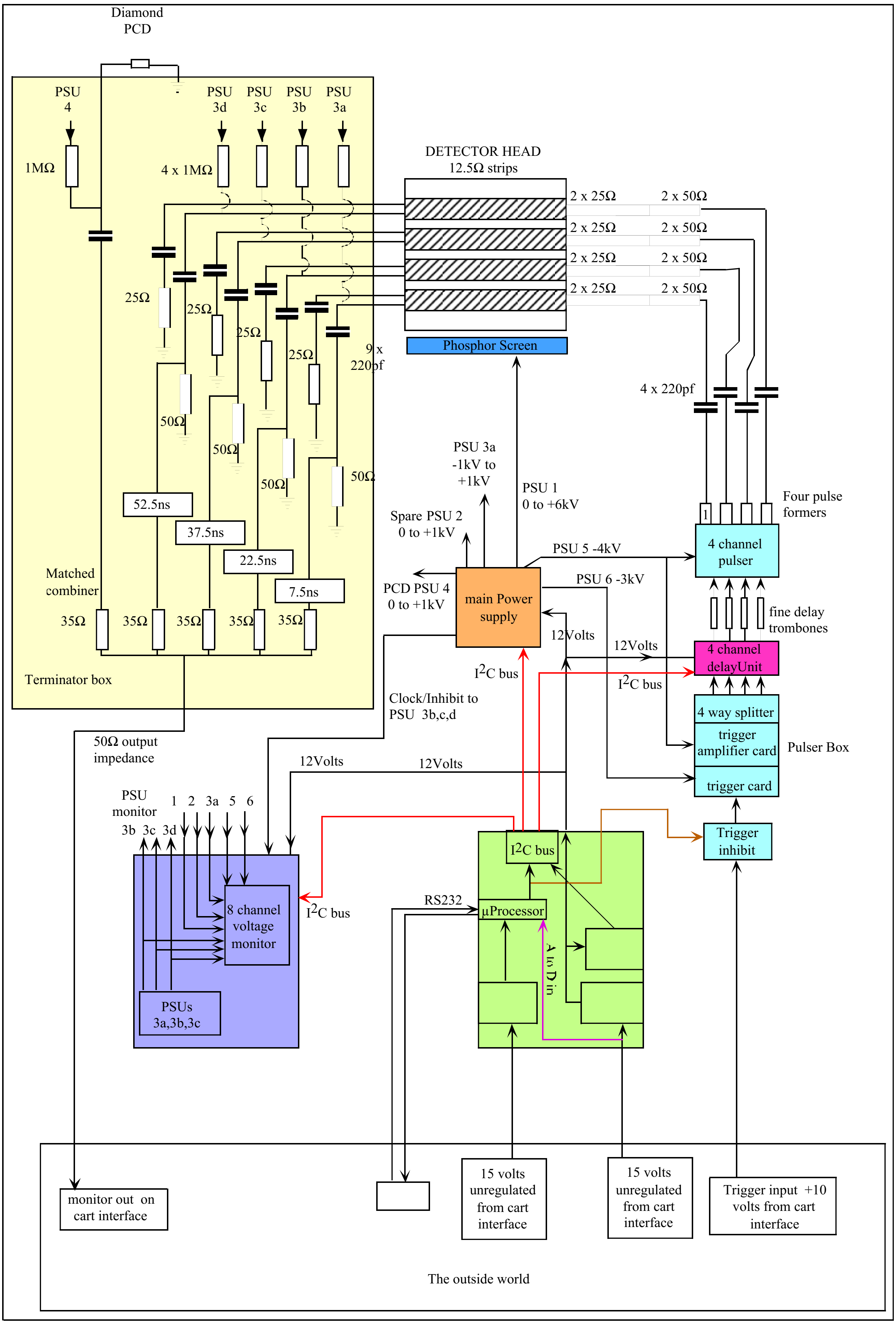



Figure 3 Layout of the main electronic components

Note that supplies 1,2,3a,4,5,6 are in the main power supply unit whilst supplies 3b,3c,3d are in the Auxiliary power supply unit. This is purely for historical reasons and if we were to redesign from scratch a different arrangement would be used.

Note that there are low voltage regulators within the computer interface. The cart actually requires two separate 15 volt unregulated supplies.

## 2.2 DELAY SECTION

Requires 12 volts fed from the computer interface box .

Current 0 to 400mA depending upon delay settings.

## 2.3 PULSE GENERATOR SECTION

Trigger input 5 to 15 volts fast rising into 50Ω

DC supplies (from power supply section) -4kV at 2mA and -3kV at 1mA.

Trigger Delay approximately 31ns at minimum delay setting

Outputs. The outputs have been set up to deliver about -6kV unshaped pulses into 50Ω. They are designed to be used with the 8 pulse forming modules supplied.

## 2.4 12VOLT REGULATORS

There are two 12 volt regulators in the computer interface box. One (main) drives the power supplies, the relays and delivers 5 volts which is used for the $I^2C$ bus. The other (μP) drives the computer only. On board regulation has been found to be necessary as long leads are usually used from a power supply to the cart and a four lead systems with sense return is too complex. Although the regulators are bolted to the body of the case it is obviously advisable to keep dissipation to a minimum by keeping the supply voltage to as low a value as maintains regulation. The software indicates if the voltage of the "main" supply is in the correct range. If very resistive power leads are used it may be necessary to increase the supplied voltage after the unit has been turned on. We recommend about 15 volts be used, up to 2.5 amps may be required. If more than around 1.5 volts is dropped in the leads to the cart there may be some problems with keeping inside the recommended operating range of input voltages for all possible settings.

## 2.5 USING THE POWER SUPPLIES

Each output on the main supply may be turned off or on individually, outputs 3b, 3c and 3d in the auxiliary power supply, follow 3a in overall control although they may have different values set. In addition the maximum voltage from each output may be set with a potentiometer, see Appendix 1. In normal use (as set at the factory) the output in question should be switched to its maximum output and then the potentiometer used to set the maximum voltage required. The indicated step voltage settings will only be accurate when the overall voltage is set to that specified above for each power supply.

## 2.7 CONNECTIONS TO THE POWER SUPPLIES.

The connections are made via Lemo connectors accessible from the bottom of the units as shown. Outputs 1, 5 and 6 which are higher voltages are on size '0' high voltage Lemo connectors. All the others and the 12 volt DC input are on size '00' Lemo connectors.


Figure 4 Clock/inhibit link

In addition there is a clock inhibit line output that goes to the auxiliary power supply to control the other three bias supplies 3b,c,d, see figure 4. By using the same clock we ensure that there is no interference between the power supplies. This is also used as the inhibit line as it is the blocking of the clock that is used in the main power supply to inhibit supplies.

There is also an $I^2C$ connector for control

Note that this particular unit has been modified to deliver 6kV on to the phosphor output (supply 1). In order to permit the use of the same connectors as for the standard 4kV units we have had to “pot” the insides of the connectors with epoxy. They have been tested to 8.5kV at sea level.

The auxiliary power supply has all the connections on one bulkhead, see figure 5. Note that this unit not only supplies power rails 3b,3c,3d but also monitors five other power rails from the main supply. For historical reasons the PCD supply is fed into the socket labelled “2in”. In fact either the PCD supply (rail 4) or the spare (Rail 2) can be used for the PCD system. If the Spare supply is used it is addressed as “SPARE” by the software in order to turn it on, off or set the voltage, but if it is connected to this “2in” connection on the auxiliary supply the PCD voltage monitor will still see it as the PCD supply. In addition there is a clock inhibit from the main power supply, a 12 volt supply and an $I^2C$ link from the computer.

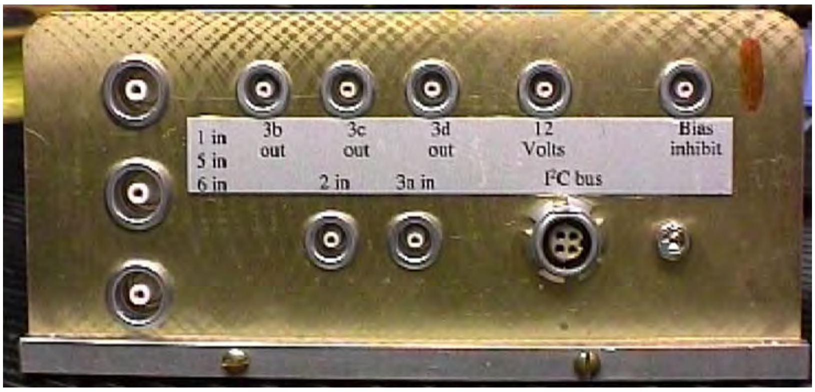



Figure 5 Auxiliary supply connector panel

## 2.8 APPLICATION

The supplies are intended for the following applications although it is for the user to use them as he or she wishes.

| | |
|---|---|
| Supply 1 | Phosphor bias |
| Supply 2 | Bias for a second MCP |
| Supply 3 a ,b,c,d | Bias supplies. |
| Supply 4 | Photodetector bias. |

The two fixed supplies drive the pulse generator. Output 5 drives the four output cards and trigger amplifier card. Output 6 drives the trigger card . The preset potentiometers for these supplies should not be adjusted.

# 3 THE PULSE GENERATOR

## 3.1 INTRODUCTION

The pulse generator provides four similar outputs from a single trigger input. It consists of several sections, a trigger card, a trigger amplifier, a four way trigger splitter, a four channel delay unit, four adjustable delay lines, four output pulse cards. The raw output from the pulse cards is then “pulse formed” by modules connected to the outputs. Pulse forming modules are available in the range 100ps to 2ns and give about half the voltage of the “raw” unshaped output. Only 100ps and 1ns modules are supplied here.

## 3.2 THE PULSER

The trigger input is via an SMA connector on the pulser bulkhead. This is fed via a trigger inhibit relay to the trigger card. This enables the trigger to be inhibited without changing the voltages on the pulser. Changing the voltages on the pulser to inhibit it can lead to changes in timing. The trigger pulse is then fed to an avalanche transistor stack to provide an output of about 2kV. This is fed to a trigger amplifier stack which delivers about 4.5kV. This is then split 4 ways with a cable transformer to give about 2.0kV into each of four channels. These trigger signals are then fed to the output cards via adjustable delay lines and a switched delay system. The switch delay circuit uses relays to switch in and out various lengths of transmission line to delay the trigger signals. The adjustable delay lines are intended to be used to compensate for small differences in the overall trigger delay of each channel or in the cabling to the load. With these controls it is then possible to have all the outputs synchronous at the loads when the delay cards are set to the same values. Note that by doing the delay control with a 2kV trigger pulse it is possible to maintain extremely low channel to channel jitter, far better than the overall trigger to output jitter.

Due to difficulty in manufacture and the fact that the delay lines are not loss free and do not have an infinite bandwidth, it will be found that the delays are not quite correct. However, they should at least be monotonic over the whole range. A calibration table is provided for unit 1.

If it is necessary to dismantle the pulser box, note that the output of the trigger amplifier card is short circuited with about 35mm of wire. This should not be disturbed. The pulse length from the trigger amplifier card is set at an optimum so that reliable triggering occurs but so that the relays in the delay section are not driven too hard.

To dismantle or re-assemble the pulser takes about ten minutes. Make sure that the various components to the box are kept around the same way as when shipped.

Note that the trigger card operates from the -3kV rail whilst the pulse cards and the trigger amplifier card operate at -4kV.

The cards have been sprayed with an insulating lacquer. This can make it difficult to work on but not impossible. Beware of solvent cleaners as they can dissolve the lacquer and make a bad mess.

On no account try to measure voltage on the board other than the -4kV at the point of connection to the board. The capacitance of probes used to measure the voltage can upset the voltage sharing and lead to a false trigger of the board. If transistors are triggered inadvertently, in this manner they are likely to fail.

If there are any suspected problems with the pulse cards they should be returned to us.

## 3.3 PULSE SHAPING MODULES

The raw pulse from each channel has a very fast edge with a slow decay. These pulses are then shaped with pulse forming modules connected to the bulkhead of the pulser unit. The pulse lengths supplied here are nominally 100ps and 1ns. There are 8 modules in all per system, four of each pulse length. Each is labelled with pulse length, the channel number and the serial number of the unit. Although all channels are intended to be identical and modules may be mixed about, it is obviously good practise to keep a note of which modules are used on which channel. This is particularly true of the 100ps modules. It has been found experimentally that electrical setting up of the gate pulse is inadequate for setting the gains of different channels identically even when gating the same strip. This is likely to be a greater effect for the short pulses.

In order to provide 100ps pulses several modifications have been made to our standard units. Firstly the pulse cards have been improved to give faster rise times and to overshoot on the rising edge. Secondly, as the BNC connectors are not adequate for 100ps use, the output bulkhead connectors are N type. Adapters to BNC are supplied so that the slower modules can be fitted and are similar to previously supplied items. When fitting the 100ps modules the BNC to N type adapters should be removed and the 100ps modules with their N type to SMA connector leads fitted instead, see figure 6. The connector leads makes the output SMAs in the same place as the slower modules.

Figure 6 100ps modules fitted


Figure 7 1ns modules fitted

When refitting the slower modules first fit the N type to BNC adapter with the “pips” horizontal. Then fit all the slow modules starting with channel 4. It is possible to mix modules, i.e. have some slow and some fast operating together.

## 3.4 CHANGING THE SLOWER PULSE FORMING MODULES

The slower modules are attached to the bulkhead on BNC connectors. As they are closely mounted they have levers fitted to help with mating the connectors, see figure 7. The levers cross over slightly and it is easier to put modules in, in the sequence 4,3,2,1, whilst taking them out in the sequence 1,2,3,4.

3.5 GATE PULSE CHARACTERISATION

This requires certain specialist equipment. In particular a suitable high voltage fast rise time attenuator, we recommend a Barth® type 142B, and a suitable oscilloscope with rise time ~ 70ps. This may be a sampling oscilloscope or fast direct access type.

When using a sampling oscilloscope considerable pretrigger is required (~ 100ns for a Tektronix 7000 system). A suitable pulse generator giving a low jitter pretrigger signal with a delay will be needed, e.g. a Kentech APG1 pulse generator.

The gate pulse generator should not be driven above 100Hz. Also the pulse generator is designed to drive the pulse forming modules and the connector interface will not take the open circuit voltage from the pulse generator. The pulse outputs must be terminated. If it is necessary to characterise the raw pulse outputs then care should be taken to stop the connectors breaking down. Normally such a breakdown will occur late after the gate pulse start. However, repetitive breaking down will eventually damage the insulators and should be avoided.

If it is necessary to investigate the raw output, bear in mind that the output voltage can rise to 7kV into 50Ω and that this will double up into an open circuit for a short time. BNC connectors can be used if carefully wired up and cables are suitably terminated.

It is possible to run the pulse cards on the bench out of the box. However, the radiated electromagnetic interference will be very high and suitable precautions with diagnostic equipment must be taken.

It has been found that even with apparently identical pulses the response of the MCP strip can still vary significantly. The gate pulse shapes are shown in figures 24, 25 and 26.

3.6 GATE PULSE TWEEKING

The 100ps pulse forming modules are simply a piece of wire shorting out the pulse generator with the self inductance of the wire. The wire diameter, length and position are all crucial to the gate pulse shape. If it is desired to modify the pulse shape the top cove of the module can be removed and the wire moved or its length changed slightly. It should be reclamped before re-characterising. With a little experience it is a simple matter to make four modules very similar.

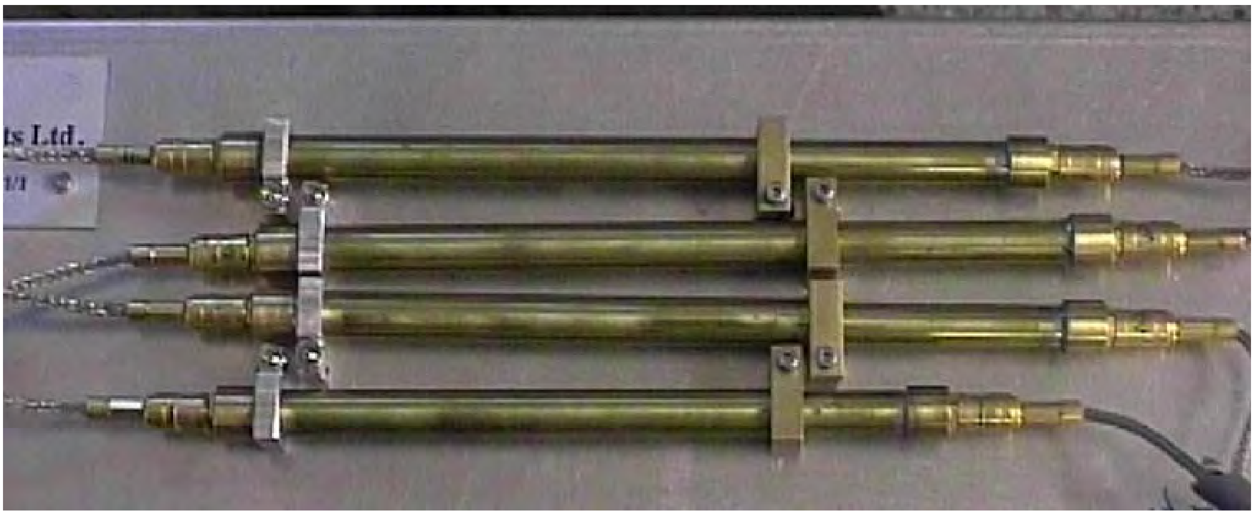



Figure 8 trigger delay trombones for synchronisation adjustment

# 4 THE DELAY UNIT

## 4.1 INTRODUCTION

The delay cards provide a nominal 12.7ns of additional delay into each channel. It is switchable in 100ps steps. In order to minimise component count and complexity the system uses seven relays per channel.

The delay cards work by switching in extra lengths of delay line into the trigger path of each signal. The bandwidth of the system is comparable to that of the trigger signal. As a result the actual delay on a channel will not be quite that expected. However, the delay should increase monotonically throughout the range. The outputs should be moderately synchronous at any delay setting as long as all four channels are set similarly.

The relays are driven directly from the supply rail. Also when a delay is "IN" the relay is energised. Consequently the maximum current is drawn when all relays are set to delay and this will be about 400mA in total at 12 volts. (Note that the high voltage power supplies take about 1.8A and the computer 0.2 A. This means that the total dissipation of the system can be 32 watts with 15 volt supplies.)

The delay period can be extended beyond 12.7ns by extending the trigger loop through leads. A male to female lead is required. SMB connectors are used for the trigger signals between the modules. More of these are available from Kentech Instruments should they not be available locally. It is important that the rise time not be degraded significantly beyond about 500ps or jitter may be introduced. With poor triggering of the output pulse cards transistor failure may occur.

The relays are powered from the regulated 12 volts DC which is fed from the computer box. The calibration of unit 1 is shown in figure 27.

## 4.2 SYNCHRONISING THE CHANNELS

The outputs of the four channels may be synchronised by adjusting the trigger delay trombones, see figure 8. When loosened, the right hand set of screws in the figure will allow the lines to be adjusted. Do not forget to retighten them. Whilst the unit is supplied with the delays synchronous at the output of the DC blocks it may be that the propagation time to the centre of the MCP strip is different on each channel (perhaps due to the use of a circular plate). The trombones will allow the user to correct for this.

Note that synchronism is only good at zero delay settings and may deviate at longer settings.

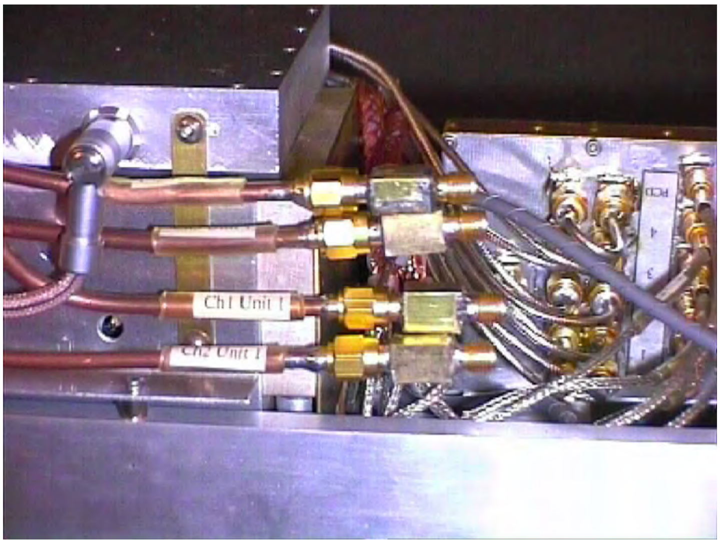



Figure 9 DC blocks

# 5 BIAS CONTROL

## 5.1 INTRODUCTION

The bias power supply provides 4 separate bias voltages each in the range -1kV to +1kV in 50 volt steps. While this offers more flexibility than earlier designs it has one drawback, the ability to place up to 2kV across the strip to strip gap on the MCP. The software prevents this being done but certain diagnostic computer commands can bypass this safety feature.

*Note that the software assumes that only adjacent channel biases are limited, e.g. with the limit set to 100 volts, one could have channel 1 on 100 volts channel 2 on 0, channel three on -100 volts etc. If the user connects channels in a different order to the bias injection circuit in the terminator it is possible that adjacent strips on the MCP could have higher voltages between them.*

The bias limit can be reset to other values in the range 0 to 1kV in 50 volt steps. This information is stored in the EEPROM and is non volatile.

## 5.2 DC BIAS BLOCKS

The DC bias blocks permit DC to be applied to the load without the bias supplies being loaded by the pulse generator. Pulse generators with pulse forming modules or with very short duration outputs have a DC path to ground.

The DC block comprises an in line capacitor of 220pF. The units have been tested for leakage current of around 1μA or less and DC hold off to >1.5kV. The pulse rise time through the DC block is around 30ps, i.e. far faster than any pulses likely to be used. The blocks are fitted along the side of the cart at present, see figure 9, but can be anywhere on the input side of the head. The bias voltage is injected via the terminator box, see figure 12.

# 6 CONNECTIONS AND MECHANICS

## 6.1 POWER UP CHECKS AND PROCEDURE

The electronics package can run at atmospheric pressure or at vacuum (better than $10^{-4}$ torr). However, the detector head can only be run under vacuum conditions and we recommend better than 5 $10^{-5}$ torr and this should be a sustained value for at least 30 minutes.

The power to the system is supplied on two 15 volt lines. One delivers power to the μ processor only. The second delivers power to the power supplies, the delay relays and to the $I^2C$ bus with which the μ processor communicates with all but monitoring of this power rail and the outside world (RS232).

## 6.2 SYSTEM PROTECTION

The power supplies and the delay unit use relays that are not designed to switch large currents but only to isolate sections. Consequently the software package will not allow these relays to be switched when there is current flowing. For the delay relays this is simply achieved by inhibiting the trigger whist delay settings are changed. Both the power supply and the delay relays require the main 12 volt rail on, in order to switch the relays on or off. Consequently commands to change the delay settings do not work with this rail unpowered; a warning message is given. Similarly the power supplies cannot be manipulated without this voltage rail powered.

The sequence for changing a bias voltage setting is

1. Test to see if the supply is enabled. If it is not permit the setting change.
2. If the supply is enabled, disable, change the setting check the main power rail and re-enable if it is above the operating threshold.

This is all done in the software automatically whenever a voltage setting is changed.

Note in addition there is a adjacent bias limit check performed when ever a bias voltage setting is made. The bias voltage on adjacent channel numbers may be pre-set so that it exceeds the bias limit but this will disable the supplies if they are enabled. The factory default of the bias limit is 200 volts but this can be changed. It is essential that in order for this protection to be effective that adjacent channels of the head are attached to adjacent channel numbers on the bias injector which is part of the terminator block.

A small problem arises if one wishes to change all bias settings from, for example, 100 volts to 1000 volts. If these are attempted one at a time then one is prevented from doing this as at intermediate steps the bias limit would be exceeded. To overcome this a 4 way bias set command is available, see the software section.

## 6.2 CONNECTING THE HEAD

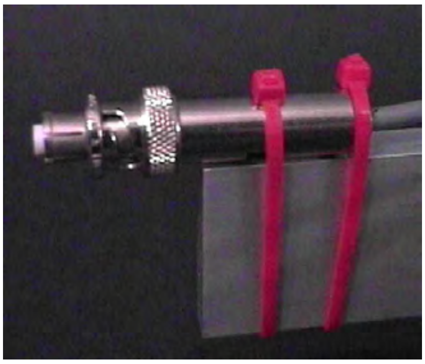


Figure 10 SHV connector for the phosphor

Connections to the head are for the Phosphor bias and the gate drive (with their individual biases also). The unit supplied has an SHV connector to connect to the head. This unit is designed to be used with a head that has four 12.5 Ω strips. Each strip is connected at each end to a pair of 25Ω cables with SMA 25 Ω jacks. 25Ω SMA connectors are difficult to obtain, however, it has been found that 50Ω connectors are not too bad especially where one wants in any case to use a mismatch.

### 6.2.1 PULSE INPUT TO THE HEAD

The pulser output is ~3kV into 50Ω. The MCP only needs around 1kV into 12.5Ω to operate. This is 4/9 of the power. Mismatches have been found to be faster than transformers except in the case of well designed exponential lines. These transformers would be prohibitively large for use with a 1ns gate pulse. By using two mismatches between the pulser and the head the *voltage* is reduced to 4/9 of the original, leaving it somewhat higher than required. This allows a higher reverse bias to be used and results in high contrast, however, the user should be aware that operation without a reverse bias will put 1.3kV on the MCP. Each mismatch has a 2:1 impedance mismatch ratio delivering 2/3 of the voltage into

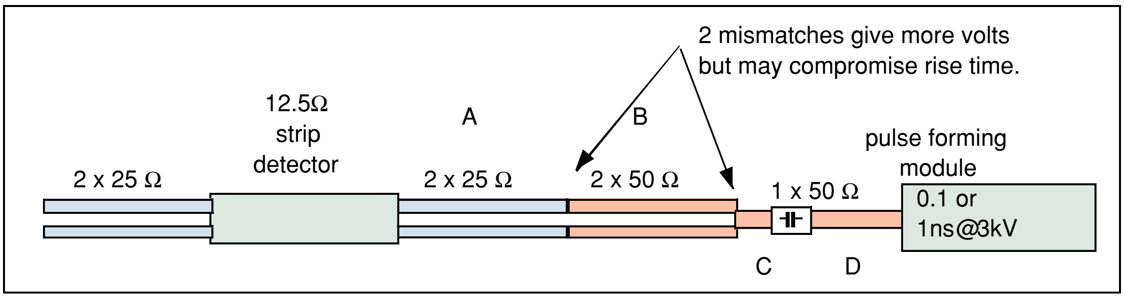



Figure 11 Input configuration to the head

the next stage. Mismatches invariably produce reflections, however, the head is normally operated with a reverse bias and also it has a very non linear response. As a result the reflections on the input side of the head are unlikely to cause any problems, see figure 14.

The unit is supplied with a set of four cables that deliver two 50Ω outputs from a single 50Ω input, section CB in figure 11. Each has two long leads, the outputs, and one short lead, the input. Connect the input to the DC block outputs and the outputs to the inputs on the head, this is where the second 2:1 mismatch occurs.

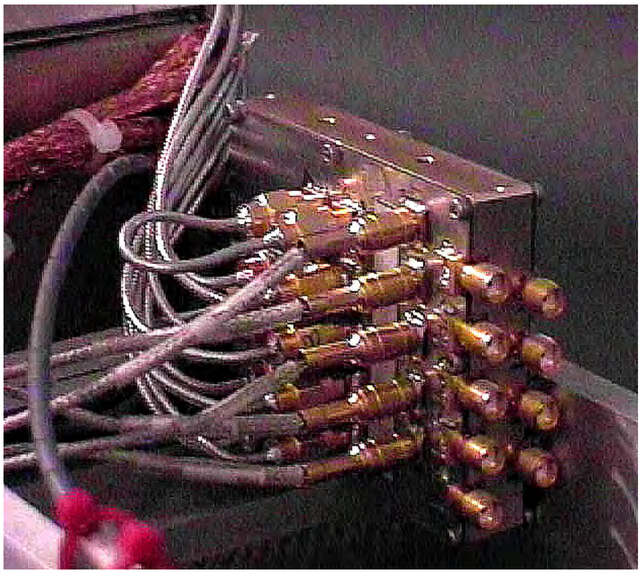


Figure 12 Terminator Block

6.2.2 PULSE OUTPUT FROM THE HEAD

On the output side one has to be a little more careful with reflections to make sure they do not re-gate the head. There are two 25Ω output leads from each strip on the detector head. These need to be connected to the terminator block. The terminator block provides four functions, 1) it terminates the pulse, preventing most of it from being reflected back to the head, 2) it allows the bias DC voltage to be applied to the head so that the gain and to some extent the pulse length can be set, 3) it provides termination and biasing for a photoconductive detector (PCD) and 4) it delays (via loop throughs) each of these five pulses (four gate pulses plus the PCD signal) by differing amounts and then sums them in a matched combiner (matched in one direction only). The output is fed off the cart.

6.3 POWERING UP THE HEAD

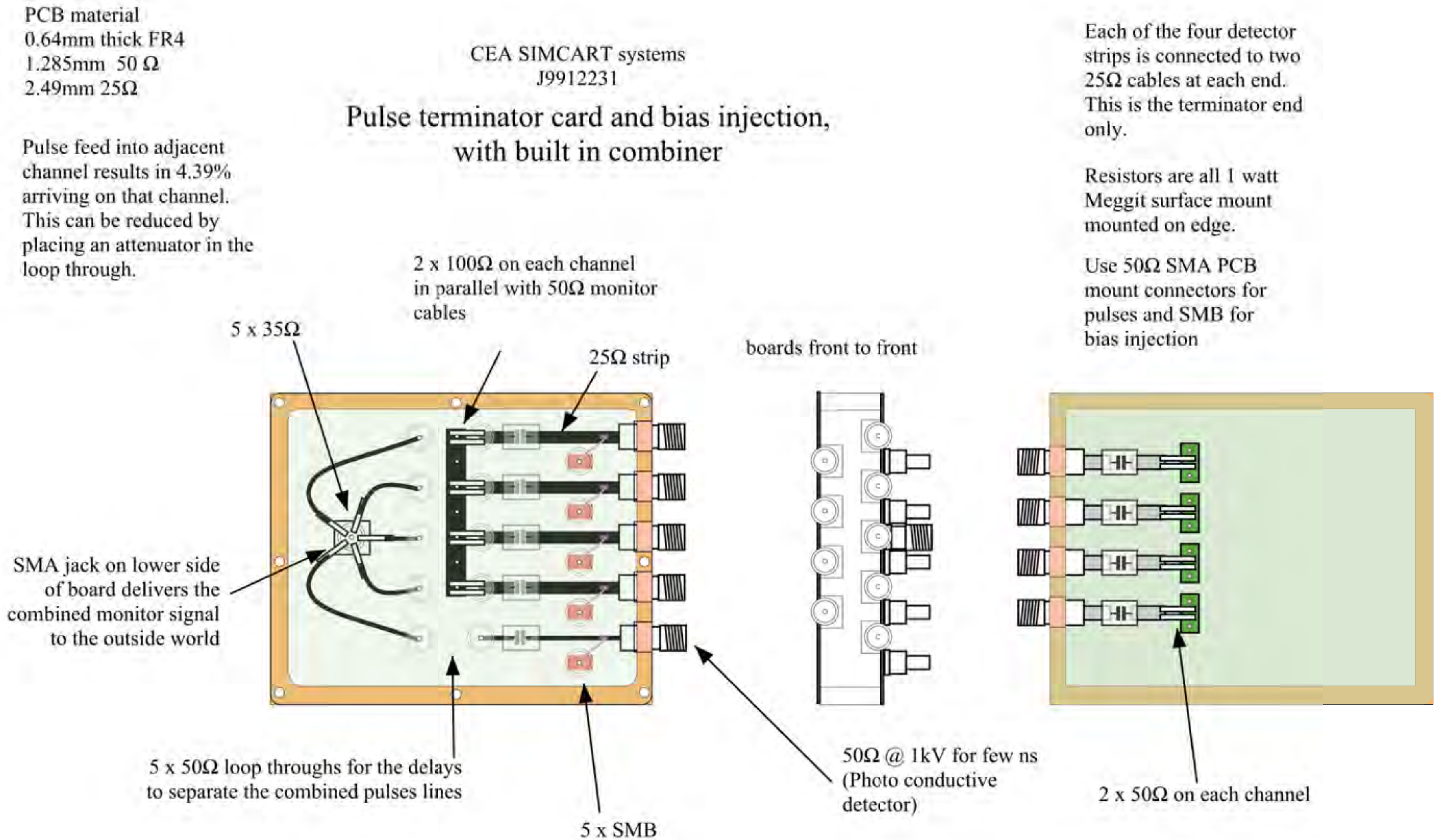
The first test that should be done under vacuum is to establish that the phosphor does not emit light when only it is powered.

With the head under vacuum and film loaded (or CCD detector active) the phosphor supply should be turned on for a little while, then off and the system removed from vacuum and the film checked for fogging. Once this test is passed it should be repeated with bias on the MCP as well. Both polarities should be checked.

With no bias voltages on the head the pulse generator monitor should be checked (also under vacuum). The monitor sums all the pulse channels with relative delays so it should be obvious if there are any problems. Both short and long pulse modules should be checked.

Once all these tests have been passed then the system can be set up for looking at x-rays. Obviously some DC shots should be performed to achieve the right gain levels on each channel. The individual channel gain can be set by adjusting the individual bias voltages.

When considering how to set the gain of individual channels one should make allowance for the relative lengths of the total x-ray emission and the gate length. Also some assumptions or calibration of the gain versus voltage on the plate needs to be made. DC calibrations will be fine for application

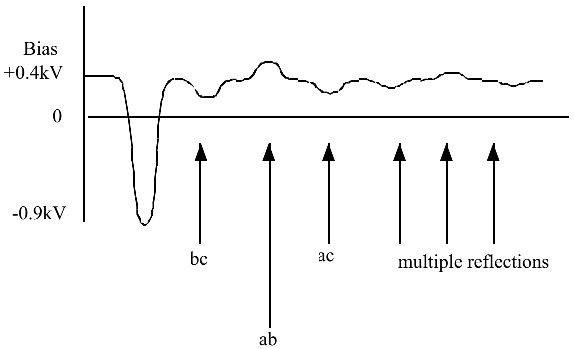



**Feed the two cables from each channel one into the biased teminator board and one to the unbiased board. The PCD drives 50Ω and only goes to the biased board.**

Figure 13 Terminator Block Details

# Reflection issues

1. The gate pulse is negative.
2. The camera is only sensitive when the total voltage on the plate is negative
3. The response of the MCP is very non linear with voltage and increases very sharply with a small increase in voltage.
4. In normal operation a positive bias is added to the pulse so that small post pulses have no effect.
5. When operating in 1ns pulse mode the reflection of a pulse from the pulser is inverted. However the 50 Ω into 25Ω also produces an inverted reflection. Similarly the 25Ω to 12.5Ω also produces an inverted reflection.
6. All first order reflections (i.e only two reflections and onto the detector strip) have the same polarity as the initial pulse.




Initial pulse
In C is -3kV
In B is -3kV x 0.67
In A is -3kV x 0.67 x 0.67 = -1.347kV

The reflection at 'b' is reflected from the pulser.
The total amplitude of this on the strip is
-3kV x (-.33) x (-.23) x 0.67 x0.67 = -0.102kV

The reflection at 'a' is reflected is reflected at 'b'.
The amplitude on the strip of this pulse is
-3kV x 0.67 x (-0.33) x 0.33 x 0.67 = +0.147kV

The reflection at 'a' is also reflected at the pulser, 'c'.
The amplitude on the strip of this pulse is
-3kV x 0.67 x (-0.33) x 1.33 x (-0.23) x 0.67 x 0.67 = -0.91kV

There are obviously many more reflections at ever decreasing amplitude

With the initial pulse at 1.347kV it wold be wise to use a bias of around +400 volts at least.
This will completely eliminate the effect of all the post pulses.
Note that if the cable length B equals the cable length C then the first two reflections coincide and the net reflection is +0.045kV still positive.

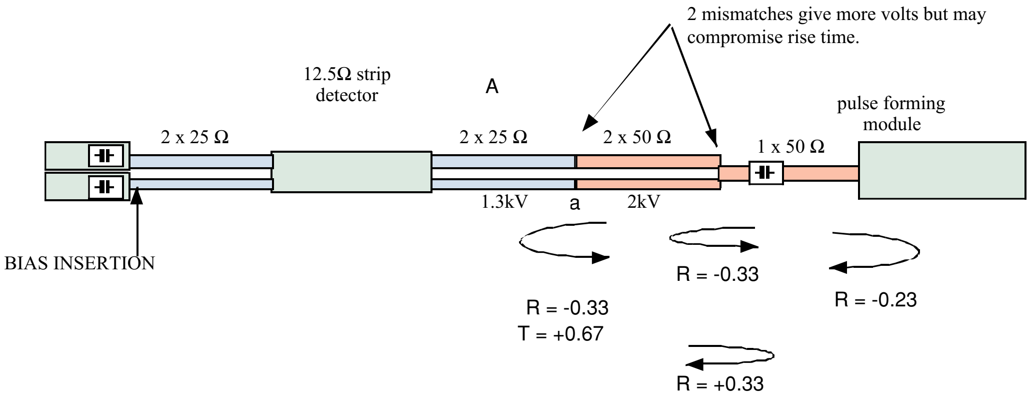



Figure 14 Reflection calculations

to the longer gate lengths. At short gate lengths the electron transit time becomes a significant fraction of the gate length and the gain at a given total voltage (bias plus gate voltage) will fall.

### 6.4 RECOMMENDED RATINGS

In order to make this unit flexible it is necessary to check that certain parameters are not exceeded. It is the users responsibility to check these. With a computer to monitor every voltage setting it is possible to prevent careless settings of the various voltage rails that could lead to component damage. The following guide lines are given on what are thought to be safe settings for heads with which we are familiar. Heads from alternative sources may have different limiting voltages and the manufacturers recommendation should be programmed into a user interface if possible to prevent accidental over setting without prior warning or the use of passwords etc. If the user keeps well below these limits they should have no problems.

**Vacuum**

Better than 5 $10^{-5}$ torr for 30 minutes

**Phosphor voltage (LLE/LLNL design)**

Lower than 3kV, start at 2.5kV and increase to 3kV after several cycles of the vacuum.

**MCP Bias (LLE/LLNL plates)**

DC bias with no gating should not exceed ±700 volts

DC bias with gating should be in the range -350 volts to +700 volts.

The peak voltage should be less than 1600 volts during gating for short gates. For longer gates keep the bias lower. Breakdown has been observed with a 2ns gate with a zero bias voltage, so it is better to use a positive bias with long gate lengths.

**Photo Conductive Detector (LLE/LLNL systems)**

Keep the voltage below 600 volts

### 6.5 TRIGGER TIMING

Once the gain has been set to an estimated value it will be necessary to set the trigger timing. By recording the output from the cart monitor it is possible to time the gate drive quickly. It is important to make sure that the PCD is illuminated with x-rays or other suitable radiation at the same time as the MCP. By using the longest gate width modules and setting the inter-frame delays to the same value a total of 4 times the gate width of the event can be monitored.

## 7 POSSIBLE FAULTS

1 MCP will not hold the bias voltage

(i) MCP plate or connections may be breaking down. Check that the MCP bias voltage is similar to that set by measuring the voltage at the bias output on the bottom of unit 4, see figure 1, with a >1GΩ voltmeter. If the MCP will not take the bias voltage then look for signs of breakdown in the various connectors and on the back of the MCP. Observe the handling conditions stated in section 1.3. Note that the SMA connectors must be able to hold off the DC bias voltage and must therefore be kept clean. In particular the insulators should be free of metal particles that come from the threads, especially on new connectors. If these threads are greased make sure to use a vacuum grease. Check out bias voltages without the head connected but with a loop from the terminator to the pulser output to check that the DC blocks are OK.

2 Phosphor will not hold bias voltage.

(i) Short circuit between MCP and phosphor. Measure impedance between Lemo centre contact and outer on the head. This should be >1GΩ.
Breakdown may be due to poor pressure (it should be better than 5 .$10^{-5}$ torr).
Look for particulate contamination of the phosphor screen or rear surface of the MCP. Observe the handling conditions stated in section 1.3.
Check to see if the MCP is bowed, if so see section 1.3.

(ii) Breakdown of EHT feed. Check without head fitted.

3 No DC image

(i) Insensitive MCP. Replace

(ii) Bad connections to MCP. Check the connections and if possible measure both the reflections from the MCP and the shape of a transmitted pulse with a T.D.R. (time domain reflectometer).

(iii) Short circuit between MCP and phosphor. Measure impedance between Lemo centre contact and outer on the head. This should be >1GΩ.

(iv) Breakdown of EHT feed.
Breakdown may be due to poor pressure (it should be better than 5 .$10^{-5}$torr).
Look for particulate contamination of the phosphor screen or rear surface of the MCP. Observe the handling conditions stated in section 1.3.
Check to see if the MCP is bowed. If so see section 1.3.

(v) MCP DC. bias not turned to negative. Switch

(vi) MCP bias too low. Increase

(vii) MCP plate or connections breaking down. If the MCP will not take the bias voltage then look for signs of breakdown on the back of the MCP. Observe the handling conditions stated in section 1.3.

(vii) Phosphor bias not on Switch on.

(viii) Phosphor bias set too low Increase

(ix) Check MCP bias lead, SMA connectors and Phosphor bias leads are mated correctly.

4 Bad focus.

(i) Image on MCP out of focus Check

(ii) Film/CCD detector contact with fibre optic faceplate is poor. Check operation of film pressure plate. Check for dirt on faceplate.

(iii) Film loaded with emulsion on wrong side. Reverse loading of film in cassette.

5 No gated image but DC image O.K.

(i) Gate drive triggering at wrong time from noise.
Block trigger diode and fire shot, electronics should not trigger.

(ii) Trigger signal not correctly timed

(iii) Gain too low

(iv) Gate leads incorrectly connected or cross connected.
SMA connectors should be tightened to a torque of 9.2 cmKg.

(v) Inadequate trigger signal causing jitter. Check with oscilloscope.

(v1) Short gate pulse module fitted but system gain set up for long pulse module

6 Image present without gate pulse.

(i) MCP bias is too high Make less negative.

(ii) Pulser is being triggered by noise at such a time that x–rays are present at the detection head when the gate pulse arrives. Improve noise immunity.

(iii) X-rays are incident at the MCP bias angle and are exciting the phosphor directly. If this happens there will be an image with the phosphor power supply turned off also.

(iv) Some other radiation e.g. neutrons or hard x-rays are exciting the phosphor directly. Remove source of radiation or improve screening.

7 Fogged film

(i) Film fogged before loading

(ii) Film not advanced sufficiently after loading.

(iii) Film advanced too quickly. The spools should be rotated slowly to avoid static problems.

8 Spurious blobs of light.

(i) Breakdown in chamber. Pressure too high.
Perform initial power up test.

(ii) Breakdown on shot. Improve the vacuum and try to stop plasma entering the detection head.

(iii) Plasma or target debris getting into MCP. It is wise to restrict the front aperture as much as possible and cover the X–ray line of sight with as thick a filter as will transmit the desired X–rays.

# 8 COMPUTER CONTROL

## 8.1 INTRODUCTION

The system uses a small embedded computer for control and monitoring. The computer is a TDS2020-PIN from Triangle Digital Services. The computer is based upon two boards fitted within the computer box, see figure 23. The computer communicates with the outside world via an RS232 bus running at 9600 baud. It also communicates with the cart via an $I^2C$ bus plus a direct analogue input on the computer itself.

Power for the computer is separated from the rest of the cart. The 15 volt input to the computer (marked μP) only supplies the processor. All other required power including the 5 volts for the $I^2C$ bus is supplied via the second 15 volt input (marked main).

## 8.2 CONTROL OF POWER SUPPLIES

The nine power supplies are driven from a common clock. The distribution of this clock is used to enable and disable each supply. Supplies 3a,b,c,d are enabled as one.

Each power supply has a feed back control loop which compares the output voltage with a reference voltage. The reference voltage is derived from a stabilised low voltage supply which is then amplified. A resistor chain in the feedback loop of this amplifier is used to set the reference voltage for each power rail. Control of the voltage is effected by shorting out resistors in this chain.

The supplies were originally designed for manual control using miniature DIP switches They have been interfaced to the $I^2C$ bus with opto isolated relays. Each relay is driven from one line of an $I^2C$ bus expander. The drive from the bus expander is via an LED which is used to help diagnose problems.

The $I^2C$ bus is buffered within each module with an $I^2C$ bus extender. This allows the $I^2C$ bus to operate over many meters. The $I^2C$ bus requires separate data and clock lines and is distributed here along with a 5 volt rail and ground. The 5 volts is derived from the main 15 volt power input. Consequently communication with the modules is only possible when both power inputs are switched on.

## 8.3 CONTROL OF THE DELAY RELAYS

The delay relays are also controlled with the $I^2C$ bus and similarly the same opto isolated relays are used to interface the delay relays to the $I^2C$ bus expander.

## 8.4 CONTROL OF THE TRIGGER INHIBIT

The trigger inhibit also runs from the $I^2C$ bus but this is connected to the bus within the computer box and a simple 5 volt output is used to control the trigger inhibit relay. The trigger inhibit relay is a double pole change over device. In the trigger active state (relay unpowered) the trigger signal is routed directly to the trigger card of the pulser. In the disabled state the trigger signal is terminated with 50Ω and the trigger input of the trigger card is also grounded via 50Ω. This greatly increases the noise immunity of the trigger circuit when disabled when compared to just disconnecting.

## 8.5 MONITORING THE VOLTAGES

Eight of the nine high voltages are monitored. The voltage is first attenuated then conditioned before being fed to an ADC connected to the $I^2C$ bus. There is no control of the attenuation or conditioning available, only a software calibration.

The main input voltage is also monitored but this is done directly by the computer on a dedicated A to D input. This enables the computer to monitor the main power input even when it is too low to operate the $I^2C$ bus.

Note that if the main power rail is off then the data acquired by the high voltage monitoring circuit is not valid. An indication of this is given by the software.

# 9 SOFTWARE

## 9.1 COMMUNICATION

The unit has an RS232 interface that runs at 9600 baud. Other speeds can be implemented, please contact us for details.

There is no hardware flow control, just read and write lines are used.

All communication is via simple text commands. The possible responses are also listed below.

The computer boots up on the application of power to the μ Processor power inlet. We recommend ~15 volts. The supply is regulated on the cart.

The computer communicates with the other components on the cart mainly via an $I^2C$ bus. This bus has two lines, Clock and Data. 5 volts regulated DC and ground are also distributed with the $I^2C$ bus.

We have found that this bus is very immune to noise from the pulser. The bus expanders in the various modules are latched decoders and encoders. Most are used as output devices but there are a couple of input bits also that can be used for diagnosis.

As these expanders can operate as input and output devices it is possible to read what has been written, this allows one to check that the bus is connected and that bits set and latched have remain latched.

There is a failure mode in that if the power to the expander ICs is interrupted (the 5 volt rail) then the latched data will be lost. Consequently the data should be written prior to every shot for normal laser target use. During fault diagnosis with the pulser being run at a significant rate this is not necessary as the noise from the pulser is insufficient to cause any problems.

The high voltages are monitored (with the exception of the spare supply number 2). The voltages are conditioned with resistive dividers and amplifiers/inverters and signals are fed to A to D convertors that are also on the $I^2C$ bus. These are less immune to noise than the digital outputs as noise can in principal get onto the voltage rails. In practice we have found that only small blips are present as voltage rails collapse slightly whist recharging the pulser after a shot. If the pulser is run at high enough repetition rates the main -4kV rail will fall and this is a good indication that the pulser is being run at too high a repetition rate.

The trigger inhibit is also driven from the $I^2C$ bus but the decoder is in the computer module with a simple 5 volt relay drive to the pulser. Note that this is active low, i.e. if the trigger inhibit lead is disconnected the unit will trigger and then cannot be inhibited with this control.

The measurement of the main power input voltage is done with an on-board (part of the computer) A to D convertor and not via the $I^2C$ bus. This allows it to monitor the voltage that delivers the 5 volts for the $I^2C$ bus.

## 9.2 COMMANDS

Note, commands preset voltages rather than set them. For preset conditions the supplies will not output these voltages until enabled.

The system is designed to prevent relays switching high voltages so that they are only used for isolation, not switching. The units with relays in are the delay circuits and the polarity switch on the bias supplies. Note that in the bias supplies there is a relay for each polarity so there are three states possible, either one on or both off (corresponding to no power applied). Consequently the supply will be inhibited until power is applied and the voltage settings established. Whenever the voltages are changed the supply is inhibited also. Similarly for the delay relays the trigger is inhibited whenever the delay is changed.

This does not apply to all the diagnostic routines, the information on which will be supplied in section 9.6 with cautions.

**We strongly recommend that the diagnostic routines do not make up any part of a user interface when the camera is being used with a head connected.**

When the "ok" is received the computer is ready for further commands.

### 9.2.1 LIST OF HIGH LEVEL COMMANDS AND THEIR EFFECT.

**`+HVPHOSPHOR`**

Turns on phosphor (1) supply, requires that the main power rail is on.

**`+HVSPARE`**

Turns on the spare (2) supply, requires that the main power rail is on.

**`+HVBIAS`**

Turns on the bias supplies (3a,3b,3c,3d), requires that the main power rail is on.

3a is connected to channel 1

3b is connected to channel 2

3c is connected to channel 3

3d is connected to channel 4

It is only possible to enable all or none of these four supplies.

**`+HVPCD`**

Turns on PCD (4) supply, requires that the main power rail is on.

**`+HVPULSER`**

Turns on pulser supplies (5&6), requires that the main power rail is on.

**`-TRIGGER`**

Disables the trigger.

**`+TRIGGER`**

Enables the trigger

The trigger state is also controlled by other functions and where possible returned to the state it was in before the function was executed.

**`-HVPHOSPHOR`**

Turns off the phosphor supply (1)

**`-HVPCD`**

Turns off the PCD supply (4)

**`-HVBIAS`**

Turns off the bias supplies (3a,3b,3c,3d)

**`-HVSPARE`**

Turns off the spare supply (2)

**-HVPULSER**

Turns off the pulser supplies (5&6)

**n !HVPHOSPHOR**

Presets the phosphor voltage supply (1) to ‘n’ volts where ‘n’ can take the values:- 750, 1500, 2250, 3000, 3750, 4500, 5250, 6000

Note these are special units for CEA and has increased phosphor voltages.

**n !HVPCD**

Presets the PCD voltage supply (4) to ‘n’ volts where ‘n’ can takes the values:- 100 to 1000 in 100 volt steps

**n !HVSPARE**

Presets the spare voltage supply (2) to ‘n’ volts where ‘n’ can takes the values: 50 to 1000 in 50 volt steps

**n !BIASLIMIT**

Sets the limit between adjacent channels to ‘n’ volts where ‘n’ takes a value 0 to 1000 in 50 volt steps. Currently set to 200 volts on boot up but changes to this value are stored in EEPROM so that they are remembered at the next boot time.

**n !HVBIAS1**
**n !HVBIAS2**
**n !HVBIAS3**
**n !HVBIAS4**

Presets the bias voltage for the relevant channel voltage supply (3a,3b,3c,3d for channels 1,2,3,4 respectively) to ‘n’ volts where ‘n’ can takes the values: -1000 to 1000 in 50 volt steps.

Although this is a “preset” command the bias can be changed once it is on. However, the software will turn the bias supplies off while the changes are made and will not turn them back on if the bias limit is exceeded with the new settings. In this case the biases cannot be turned on until the settings are modified and no longer exceed the bias limit. If the bias limit is reduced, causing it to be exceeded by the current settings, the bias supplies will be disabled.

Note the bias limit conditions may turn off the bias supply if for example one tried to increase all the settings by 500 volts and the limit was set at 200 volts. This is because the voltages are changed one at a time, this limitation is overcome with the following command.

**a b c d !HVBIAS1234**

Where a,b,c,d are the bias voltages for channels 1,2,3,4 respectively. a,b,c,d may range from -1000 to +1000 volts in 50 volt steps and adjacent bias voltages must not exceed the bias limit.

This command will set all the biases in one go. As the bias is turned off while the change is made, at no time will the voltage exceed the bias limit if the values of a,b,c,d do not themselves exceed the limit.

**n !DELAY1**
**n !DELAY2**
**n !DELAY3**
**n !DELAY4**

Sets the delay of the relevant channel to 'n' picoseconds. For this unit 'n' may take any value from 0 to 12700 in steps of 100.

The EEPROM has stored in it whether the system uses a 100 ps step 12.7ns delay unit or a 50 ps step 6.35ns delay unit. Consequently the delay unit may be swapped if the relevant command is issued to modify the EEPROM (see calibration, section 9.6).

**a b c d !DELAY1234**

This sets all the delays in one go. 'a,b,c,d' are in picoseconds. For this unit 'n' may take any value from 0 to 12700 in steps of 100.

**SAFE**

Sets all power supplies to OFF

**MINIMUM**

Sets all voltages to lowest possible.

**?STATUS**

Displays the current set of all parameters and voltages.

**?SERIAL#**

Displays the serial number of the instrument as set by the serial number writer command, see section 9.3.

**?VERSION#**

Displays the Software version number

**8574DATA>HW**

Re-sends the stored data (as defined by voltage setting commands) to the latches. Use this command if ?STATUS indicates a failed latched data read back test after a shot and the settings are required to be the same for the next shot. If the status indicates a failure without a shot then there is a hardware failure of some type.

**+RECORDING** and **-RECORDING**

+RECORDING starts the unit recording the voltages on the eight high voltage power supply rails that are monitored (i.e. not the Spare) and the regulator input voltage. This will record these settings every 500 ms until a -RECORDING is received. This will record a maximum number of 512 records. After 512 the earlier ones are over written continuously leaving only the last 512 records.

This process runs in the background and does not prevent other commands from being issued.

**?#RECORDS**

This returns the number of records taken during a recording session.

**DUMPRECORDS**

This will send the records to the host. The last record made will be the first sent. Each record is marked with a "TICK" number to indicate its position in time. Ticks are in units of 53.3446ms and are derived from the computer clock. They start at an arbitrary number, lower numbers are earlier.

NOTE:- if the regulator supply voltage is too low the data on the high voltage supply measurements will be meaningless.

**RECORDTITLE**

The puts a title above a record dump to indicate the parameter that has been measured. Note that to have the titles directly above the record data the two commands should be strung together to avoid the intermediate response to the first command,

e.g. **RECORDTITLE DUMPRECORDS** *cr*

9.3 SETTING THE SERIAL NUMBER OF THE UNIT

This is achieved with a special serial number writer command. To set the serial number to a character string of up to 32 characters with no spaces, type the following:-

YOU'RE The_Serial_Number *cr*

where "The_Serial_Number" is the serial number to be written.

9.4 THE LANGUAGE

The software that is used in the cart computer is FORTH. This is an ideal language for machine control (Postscript is based upon it). The user does not have to be aware of this except to understand how commands may be strung together and simple macros defined and executed.

The system uses a stack that has on the top the last item entered.

For example to set the bias voltages to -50, 0,50,100 on channels 1 through 4 respectively one could enter:-

**-50 !HVBIAS1 *cr* ok**
**0 !HVBIAS2 *cr* ok**
**50 !HVBIAS3 *cr* ok**
**100 !HVBIAS4 *cr* ok**

where *cr* is a carriage return entered by the user and ok is the machine response.

Alternatively one could enter

**-50 0 50 100 !HVBIAS1 !HVBIAS2 !HVBIAS3 !HVBIAS4 *cr* ok**

If one wants to flip between several settings then a macro could be used to set up each state.

Macros are defined with a command string that starts with a colon ":" followed by a space and then the name. Forth is case sensitive. The macro must finish with a space followed by a semicolon. Commands or data should be delimited by spaces or "cr"

e.g.

**: STATE1 -50 0 50 100 !HVBIAS1 !HVBIAS2 !HVBIAS3 !HVBIAS4 +HVBIAS ;*cr* ok**

**: STATE2 50 100 50 150 !HVBIAS1234 +HVBIAS ;*cr* ok**

**: STATE3**
**50 100 50 150**
**!HVBIAS1234**
**+HVBIAS ;*cr* ok**

Macros can be redefined and the last definition is the one used, however, if macroA contains macroB and then if macro B is redefined, macro A will still contain the old definition.

Where one has repeatedly to enter a long command name by hand it is often simple to define a new simply named macro that calls the long named one. However, for ease of long term use it is desirable to have macro names that describe the function adequately.

e.g.

**: S3 STATE3 ;*cr* ok**

this will make the entry of S3 do the same as STATE3

Macros entered in this way will be lost from the computer's memory on shut down. It is a good idea to keep a file with all the definitions in that can be sent to the machine to reinstate them.

## 9.5 POWERING UP/REBOOTING THE COMPUTER.

Whilst the computer is powered from the μ processor power inlet it also monitors the voltage on the main power inlet that is used for the power supplies. In order to protect the computer from too high a voltage on this rail there are diodes that limit the voltage. However, when the μ processor power is off, enough current can leak through these diodes to keep the memory of the computer alive (or possibly partially corrupted). When rebooting the computer make sure the main power if off when the computer is switched back on. This will ensure that the memory cannot be kept alive by this leakage current.

## 9.6 DIAGNOSTIC ROUTINES (MACROS)

Do not use these diagnostic routines as part of normal operations. Safety checks are not carried out with many of them. Also these commands do not all save a local copy of the data that is sent to the latches. Consequently a ?STATUS command will return a fault condition.

The following is a list of routines that we have found useful in checking out the units.

**CR**

Outputs a carriage return, useful for formatting.

**KEYWAIT**

This command will cause the computer to wait for any key to be hit (character to be sent).

**?KEY**

Puts 1 on the stack if a key is pressed, else 0.

This can be used to allow the user to stop infinite loops

e.g.

**: SET4KV +PS4KV BEGIN 10 0 DO @AD4KV . 200 MS LOOP CR ?KEY UNTIL SAFE ;**

This macro called SET4KV turns on the -4kv rail to the pulser without doing any checks and enters an infinite loop. Within the loop the -4kV rail is read and sent to the RS232 port; the '.' does this. A delay is added to limit the speed round the loop and the loop tests for a character to be entered to exit the loop. On leaving the loop the system is made safe with the "SAFE" command.

**PHOSTEST**

Steps through the phosphor voltages. Each voltage is held for 5 seconds to allow DMM reading. Phosphor is switched OFF at the end of the test.

**Make sure it is OK to turn ON the phosphor voltage to its maximum value" No checks are made . Do not use this command unless you are sure this is what is needed.**

**ALLON**

Switches all the delay relays on

**ALLOFF**

Switches all the delay relays off

**READ_RELAYS**

Reads the delay settings in units of 100ps (not steps)

The output format is:-

```
CH1   63
CH1   32
CH1   29
CH1   109
```

**n MS**

Waits approximately n milliseconds, this is particularly useful for allowing power supplies or relays to settle.

**DELAYRIP**

Delay relay testing routine. Listen for 28 clicks of the relays turning on. All relays are set to off before and after the test. READ_RELAYS is executed after each one is turned on.

This is an ideal routine for checking for duff delay relays. The human ear is very sensitive to changes in periodic sound, far better than the eye. It is not possible for the computer to check that a relay has been activated. However, by listening for a missing click one can immediately tell if all the relays are working. Note that all relays are initially set to OFF then the test starts 2 seconds later. At the end off the test there is a 2 second wait before they are all turned back off. Very occasionally a relay can fail even though it clicks well. If this is suspected one has to look at the pulser timing directly.

**Do not use this routine with the pulser running as it has no trigger inhibit protection.**

**PCDTEST**

Steps through the PCD voltages. Each voltage is held for 3 seconds to allow DMM reading. PCD is switched OFF at the end of the test. Make sure it is OK to turn ON the PCD voltage to its maximum value before executing the test. This displays the calibrated voltages. No checks are made . Do not use this command unless you are sure this is what is needed.

**POWERTEST**

Displays the APPROXIMATE main input voltage continuously in units of 100mV

HIT ANY KEY TO STOP

**LISTBIAS**

This lists the bias counts, note 127 ~ 0 volts, the range is from 0 to 255. The output format is:-

```
CH1   63
CH1   32
CH1   29
CH1   109
```

**LISTBIAS2**

As LISTBIAS but the output format is as follows:-

63   32   29   109

These are TAB delimited in the same order as LISTBIAS

**LISTBIAS3**

This outputs as LISTBIAS2 but in mV

LISTBIAS3 + 205 |+ 254 |+ 154 |+ 203

**BIASTEST**

Steps through bias voltages all channels move together.

Make sure it is safe to have biases at any voltage. The settings are held for 3 seconds to permit use of a DMM. The voltages are output by **LISTBIAS3.**

No checks are made . Do not use this command unless you are sure this is what is needed. To check that the bias channels are wired up correctly set the bias voltages to different values and measure the outputs on the SMA connectors to the head, with a DVM.

**SPARETEST**

Steps through the spare supply (4) voltages. These are not monitored by the cart. No checks are made . Do not use this command unless you are sure this is what is needed.

**+PS3KV**

Turns on the -3kV power to the pulser trigger card. No checks are made. Do not use this command unless you are sure this is what is needed.

**+PS4KV**

Turns on the -4kV power to the pulser output and trigger distribution cards. No checks are made . Do not use this command unless you are sure this is what is needed.

**-PS3KV AND -PS4KV**

Turns the -3kV and -4kV supplies off.

**SET3KV**

This turns on the -3kV supply (6) and continuously displays the count from the A to D.

To stop the listing hit any key. This will then execute a SAFE command. Set3KV is useful when setting up the -3kV voltage. No checks are made. Do not use this command unless you are sure this is what is needed.

**SET4KV**

As SET3KV but for the -4kV (5) supply. No checks are made. Do not use this command unless you are sure this is what is needed.

**MAINPSUOK**
**AUXPSUOK**
**DELAYBOXOK**

These routines compare the data in the hardware latches with the data in RAM that should have been written to them. Each command returns a 1 to the stack if the data agree and a 0 if it does not. They can be used to check communication with the hardware and also to establish if the data has been corrupted in the latches by EMP. Latches can reset themselves if the power is interrupted. To print the item on top of the stack enter a "." followed by a carriage return.

For example if one does not have time to read a full status report but wants to check that the data is latched properly one could define a "simple status" macro:-

: SS AUXPSUOK? MAINPSUOK? AND DELAYBOXOK? AND . ;

Send this line to the unit. Then to do a "simple status" test just send SS. If the reply is 1 tests are OK if a zero it is not. This command will not be remembered when the power is turned off.

## 9.7 TYPICAL RESPONSES

The following is a list of typical responses that a terminal would receive from the system.

**+HVPHOSPHOR**

```
? - Power input voltage too low ok
```

+HVPHOSPHOR **ok**

The response from the other commands that turn on power supplies are similar.

**+HVBIAS**

This can respond differently if the bias limit is exceeded. The following is a sequence of dialogue with the cart.

```
200 !BIASLIMIT  ok
100 200 300 600 !HVBIAS1234
* - Bias settings now exceed bias limit, bias supplies are OFF ok
+HVBIAS
? - Bias limit exceeded ok
1000 !BIASLIMIT  ok
+HVBIAS  ok
200 !BIASLIMIT
* - Bias settings now exceed bias limit, bias supplies are OFF ok
+TRIGGER
The response to this will depend upon the state the cart is in, e.g.:-
+TRIGGER
? - Bias limit exceeded
? - Pulser power supply not enabled ok
0 0 0 0 !HVBIAS1234  ok
+TRIGGER
? - Pulser power supply not enabled ok
+HVPULSER  ok
+TRIGGER  ok
```

**?STATUS**

The following is a typical response:-

```
Serial No. = XRFC1_Software_19th.June_2000

Cart supply =    14627mV   - within correct range
Bias limit set =  1000V     Bias limit flag =    OFF

Phosphor supply = ON   Set value =      4000V   Measured value = 3966V
PCD supply =      ON   Set value =      1000V   Measured value =  994V
Spare supply =    ON   Set value =      1000V
Pulser supply =   ON   Measured value = 4083V
Trigger supply =  ON   Measured value = 3050V

Bias supplies =   ON
Bias1 set value = + 100V Measured value = + 100V
Bias2 set value = + 200V Measured value = + 206V
Bias3 set value = + 300V Measured value = + 300V
Bias4 set value = + 400V Measured value = + 397V
```

```
Delays (ps) are
set to and measured as
6000      6000
6000      6000
6000      6000
6000      6000

Latched data read back test:-
Delay box Passed
Main psu  Passed
Aux psu   Passed ok
```

If there are problems with the main cart supply one of the following two headers will be received, the exact figures will depend upon the voltage measured.

```
Cart supply =    20186mV * - too high, excessive power dissipation
                             use 14375 to 16000mV
or
Cart supply =    12271mV ? - too low to operate use 14375 to 16000mV
                 measured high voltages are not true
```

The last line of the ?STATUS command response indicates that the hardware control latches have the data in them that was last written. If the data in the latches does not agree with the data that was last sent then the response on the is last lines are

```
FAULT ok
```

This implies that either there is a communication error between the embedded computer and the hardware or the contents of the latch has been lost. We have checked that latches retain the data when the pulser fires, even repeatedly. However, in more extreme environments it is possible that the latched data could be corrupted. Whilst it is unlikely that data can be entered into the latch it is possible that a glitch on a power or control rail could cause the latches to reset making everything high (inactive).

Some of the diagnostic routines do not store the data locally but just write to the latches. So if one has executed a DELAYRIP for example then the ?STATUS command will indicate a FAULT unless the delays happen to be set to zero by the !DELAY commands. Do not use the diagnostic routines for general use.

The obvious solution is to write the data before every shot. This can be done from the terminal or alternatively by executing a **8574DATA>HW** command. This re-sends all the data to the latches. If this does not restore the latched data and a fault state is still indicated then there is a real fault.

**?#RECORDS**

```
No of records = 8
```

**RECORDTITLE DUMPRECORDS**

The response is as shown below, remember that if the regulator supply is low then the measured high voltages are meaningless.

```
TICK   PHOS   ———BIAS 1 THROUGH 4———        PCD   4KV    3KV    REG IN

 4749    12   +   2  +   3  +   5  +   7   994     45     86   15924
 4739    12   +   2  +   3  +   5  +   7   994     45     86   15924
 4730    12   +   2  +   3  +   5  +   7   994     45     86   15883
 4643    12   +   2  +   3  +   5  +   7     1     45     86   15924
 4634    12   +   2  +   3  +   5  +   7     1     45     86   15883
 4624    12   +   2  +   3  +   5  +   7     1     45     86   15903
 4615  4029   +1032  +1044  +1055  +1039   994     45     86     498
 4605  4029   +1032  +1044  +1055  +1039   994     45     86     477
 ok
```

**PCDTEST**

The response will be

```
Steps through the PCD voltages
Each voltage is held for 5 seconds to allow DMM reading
PCD is switched OFF at the end of the test

——— DANGER ———

Make sure it is OK to turn ON the PCD voltage to its maximum value
Hit any to continue

Volts
  99 201 298 400 501 603 701 802 904 994

PCD OFF reading = 4 Volts
 ok
```

## 9.6 CALIBRATION

The calibration for the voltages along with a few other parameters are stored in an EEPROM. As such they can be changed by the user and are non volatile.

The calibration supplied with the unit is one of the following, see the serial number on the unit to find which is relevant.:-

```
: TBCAL ( - CALIBRATION DATA FOR CEA_UNIT1_J9912231/1 8-11-2000 -)

 (  - [COUNT * J1/J2]+J3 = VOLTAGE [OR mV FOR 12 VOLT RAIL] except for -4 and -
3kV rails which need the measured voltages reversed)

( - J1    J2    J3    item to be calibrated  )
23646 1000  -36 'CALPHOS      !CAL
3894  1000  -1    'CALPCD     !CAL
8014  1000  -1011 'CALBIAS1+  !CAL
8050  1000  -1023 'CALBIAS1-  !CAL
8050  1000  -1020 'CALBIAS2+  !CAL
8064  1000  -1015 'CALBIAS2-  !CAL
8141  1000  -1038 'CALBIAS3+  !CAL
8062  1000  -1023 'CALBIAS3-  !CAL
8062  1000  -1011 'CALBIAS4+  !CAL
8004  1000  -1014 'CALBIAS4-  !CAL
-15888      1000  4064  'CAL4KV     !CAL
-11960      1000  3048  'CAL3KV     !CAL
22474 1000  -2789 'CAL12V     !CAL
```

```
   840 PSHI Nv!   ( - High voltage for 15 volt supply set to around ~ 16000mV )
   769 PSLO Nv!  ( - Low voltage for 15 volt supply set to around ~ 14375mV )

   4 'BIASLIMIT# Nv!  ( - 1 UNIT = 50 VOLTS  RANGE 1 TO 20)

   500 RECORDMS Nv!  ( - time between records in record mode )
   100PSUNIT   ( - Sets up the software so that it will drive a 100ps per step
delay unit )
                  ( - To drive a 50ps step delay unit send the command 50PSUNIT
instead )
   ;


: TBCAL ( - CALIBRATION DATA FOR CEA_UNIT2_J9912231/2 18-10-2000 -)

 (  - [COUNT * J1/J2]+J3 = VOLTAGE [OR mV FOR 12 VOLT RAIL] except for -4 and -
3kV rails which need the measured voltages reversed)

 ( - J1    J2    J3    item to be calibrated  )
23807 1000  1      'CALPHOS    !CAL
3855  1000  0      'CALPCD     !CAL
8099  1000  -1020 'CALBIAS1+  !CAL
8040  1000  -1016 'CALBIAS1-  !CAL
8042  1000  -1027 'CALBIAS2+  !CAL
7998  1000  -1012 'CALBIAS2-  !CAL
8075  1000  -1015 'CALBIAS3+  !CAL
7991  1000  -1010 'CALBIAS3-  !CAL
7997  1000  -1005 'CALBIAS4+  !CAL
8075  1000  -1021 'CALBIAS4-  !CAL
-15940      1000  4065  'CAL4KV     !CAL
-11905      1000  3037  'CAL3KV     !CAL
22222 1000  -2866 'CAL12V     !CAL

   840 PSHI Nv!   ( - High voltage for 15 volt supply set to around ~ 16000mV )
   769 PSLO Nv!  ( - Low voltage for 15 volt supply set to around ~ 14375mV )

   4 'BIASLIMIT# Nv!  ( - 1 UNIT = 50 VOLTS  RANGE 1 TO 20)

   500 RECORDMS Nv!  ( - time between records in record mode )
   100PSUNIT   ( - Sets up the software so that it will drive a 100ps per step
delay unit )
                  ( - To drive a 50ps step delay unit send the command 50PSUNIT
instead )
   ;
```

In order to change the calibration there are a few steps,

1) calculate the new calibration in terms of the three numbers J1, J2 and J3 as defined above.

2) Edit a file so that it looks like the one listed here but with the new values of the calibration. Do not forget the final ';'

3) Send the file to the unit, await the ok response.

4) Send the command TBCAL to execute the file.

Alternatively one can send each calibration line individually without the header definition. In this case that is all one has to do.

## 9.7 COMMANDS TO HELP WITH ESTIMATING A NEW CALIBRATION

For each voltage rail in turn

Set rail to a non zero (in case of underflow) low voltage, measure the voltage with a probe execute a command (see below) to give the count from the ADC

Set the voltage high but not at maximum (in case of overflow) measure the voltage with a probe execute a command to give the count from the ADC.

You now have four numbers $V_{low}$, $C_{low}$, $V_{high}$, $C_{high}$.

Calculate J1 and J3 (J2 = 1000)

$J1 = 1000 *(V_{high} - V_{low})/(C_{high} - C_{low})$

$J3 = V_{high} - C_{high} (J1/J2)$

Make sure you use the correct the signs of the voltages in the equation for all except supplies 5 and 6 which are defined with the above equation only if the wrong sign is put in for the measured value. (Programmer was not thinking straight.)

Edit the TBCAL file with the new values for J1 and J3 and send it to the unit. Send the command TBCAL and the data will be stored in the EEPROM and implemented.

Note that for the bias voltages there are separate calibrations for positive and negative. Counts of 0 to 127 use the negative and 128 to 255 use the positive calibrations.

To read counts use the following commands:-

@ADPHOSPHOR .

@ADPCD .

LISTBIAS (this lists all four as per manual)

@AD4KV .

@AD3KV .

Note that there is a space before the periods. The period means send the item on top of the stack to the RS232 port.

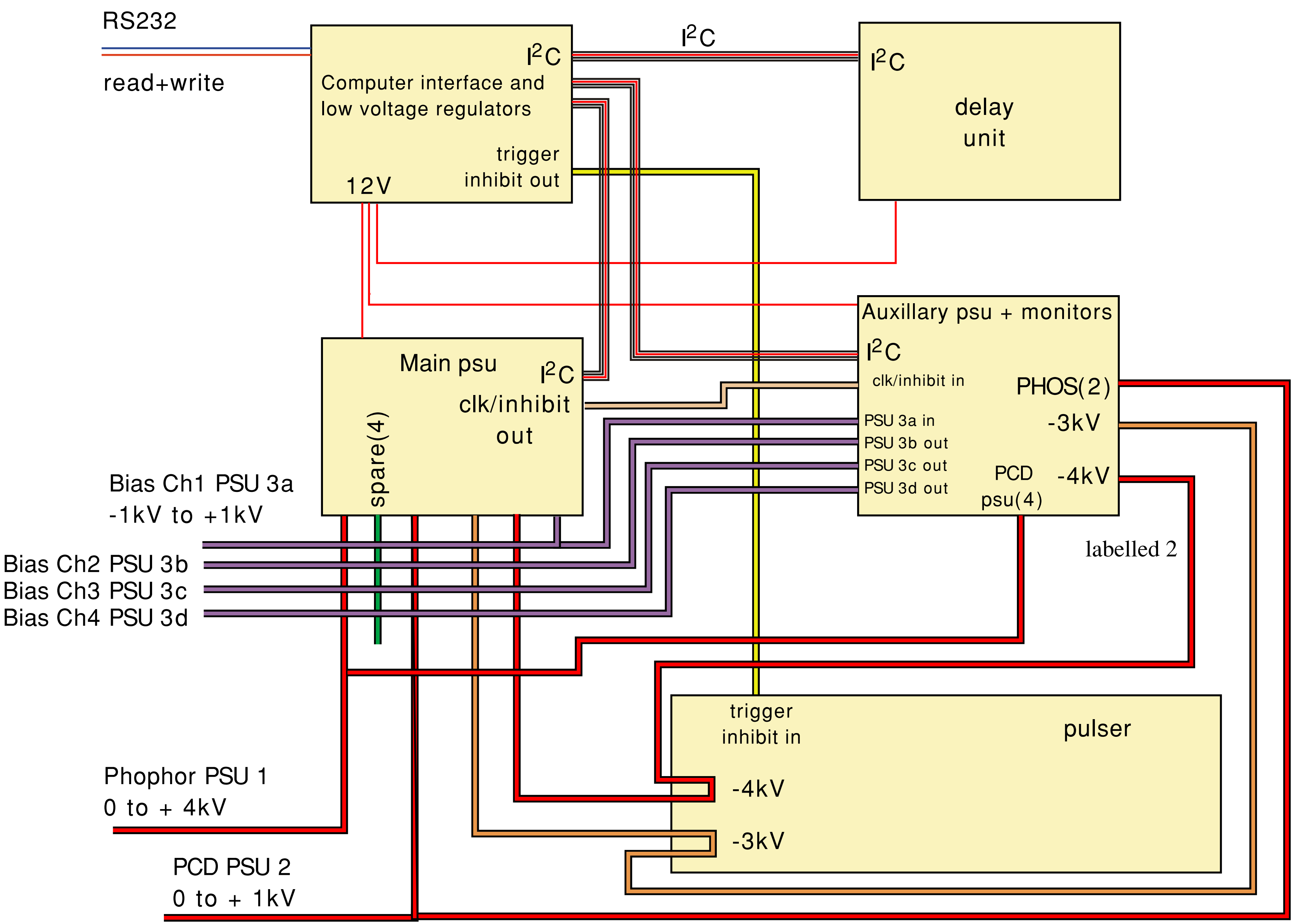



Figure 15 General layout of controls and monitoring

# $I^2C$ addresses

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | bit | lsb =0 | msb=7 | | | |
| **use** | **power supplies** | **operation** | **sense** | **address** | **bit** | | | | | |
| phosphor | 1 | on/off | Lo = ON | 0 | 0 | | | | | |
| spare | 2 | on/off | Lo = ON | 0 | 1 | | | | | |
| ch1 bias | 3a | on/off | Lo = ON | 0 | 2 | | | | | |
| ch2 bias | 3b | on/off | Lo = ON | 0 | 2 | | | | | |
| ch3 bias | 3c | on/off | Lo = ON | 0 | 2 | | | | | |
| ch 4 bias | 3d | on/off | Lo = ON | 0 | 2 | | | | | |
| PCD | 4 | on/off | Lo = ON | 0 | 3 | | | | | |
| pulser -4kV | 5 | on/off | Lo = ON | 0 | 4 | | | | | |
| pulser -3kV | 6 | on/off | Lo = ON | 0 | 5 | | | | | |
| | | | | | | | | | | |
| **phosphor** | **power supply 1** | **control bits** | | | | | **voltage** | | | |
| | with no control bits | 750 | Hi = add 750 V | 1 | 0 | | 0 | set off | | |
| | set this voltage is 500 volts | 1500 | Hi = add 1500 V | 1 | 1 | | 750 | set on | | |
| | | 3000 | Hi = add 3000 V | 1 | 2 | | 1500 | set On | + | 0 |
| | | | | | | | 2250 | set On | + | 1 |
| | | | | | | | 3000 | set On | + | 0,1 |
| | | | | | | | 3750 | set On | + | 2 |
| | | | | | | | 4500 | set On | + | 2,0 |
| | | | | | | | 5250 | set On | + | 2,1 |
| | | | | | | | 6000 | set On | + | 2,1,0 |
| | | | | | | | | | | |
| **Spare** | **Power supply 2** | **control bits** | | | | | **voltage** | | | **set bits hi** |
| | | 50 | Hi = add 50 V | 1 | 3 | | 0 | set off | | |
| | | 100 | Hi = add 100 V | 1 | 4 | | 50 | set on | | 3 |
| | | 200 | Hi = add 200 V | 1 | 5 | | 100 | set on | | 4 |
| | | 250 | Hi = add 250 V | 1 | 6 | | 150 | set on | | 3,4 |
| | | 400 | Hi = add 400 V | 1 | 7 | | 200 | set on | | 5 |
| | | | | | | | 250 | set on | | 5,3 |
| | | | | | | | 300 | set on | | 5,4 |
| | | | | | | | 350 | set on | | 6,4 |
| | | | | | | | 400 | set on | | 7 |
| | | | | | | | 450 | set on | | 7,3 |
| | | | | | | | 500 | set on | | 7,4 |
| | | | | | | | 550 | set on | | 7,4,3 |
| | | | | | | | 600 | set on | | 7,5 |
| | | | | | | | 650 | set on | | 7,6 |
| | | | | | | | 700 | set on | | 7,5,4 |
| | | | | | | | 750 | set on | | 7,6,4 |
| | | | | | | | 800 | set on | | 7,6,4,3 |
| | | | | | | | 850 | set on | | 7,6,5 |
| | | | | | | | 900 | set on | | 7,6,5,3 |
| | | | | | | | 950 | set on | | 7,6,5,4 |
| | | | | | | | 1000 | set on | | 7,6,5,4,3 |

Figure 16 $I^2C$ addresses

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | |
| **Ch1 Bias** | **power supply 3a** | **control bits** | | | | | **voltage** | | | **set bits hi** | | | |
| Do not set OFF for 0 volts as this will turn off the bias on the other channels also. | | | | | | | | | | | | | |
| | | ± | Hi = negative | 3 | 0 | | -1000 | set on | | 0,1,2,3,4,5 | | | |
| | | 50 | hi = add 50 V | 3 | 5 | | -950 | set on | | 0,1,2,3,4 | | | |
| | | 100 | hi = add 100 V | 3 | 4 | | -900 | set on | | 0,1,2,3,5 | | | |
| | | 150 | hi = add 150 V | 3 | 3 | | -850 | set on | | 0,1,2,3 | | | |
| | | 200 | hi = add 200 V | 3 | 2 | | -800 | set on | | 0,1,2,4 | | | |
| | | 500 | hi = add 500 V | 3 | 1 | | -750 | set on | | 0,1,2,5 | | | |
| | | | | | | | -700 | set on | | 0,1,2 | | | |
| | | | | | | | -650 | set on | | 0,1,3 | | | |
| | | | | | | | -600 | set on | | 0,1,4 | | | |
| | | | | | | | -550 | set on | | 0,1,5 | | | |
| **Ch2 Bias** | **power supply 3b** | **control bits** | | | | | -500 | set on | | 0,1 | | | |
| Do not set OFF for 0 volts as this will turn off the bias on the other channels also. | | | | | | | -450 | set on | | 0,2,3,4 | | | |
| | | ± | Hi = negative | 4 | 0 | | -400 | set on | | 0,2,3,5 | | | |
| | | 50 | hi = add 50 V | 4 | 5 | | -350 | set on | | 0,2,3 | | | |
| | | 100 | hi = add 100 V | 4 | 4 | | -300 | set on | | 0,2,4 | | | |
| | | 150 | hi = add 150 V | 4 | 3 | | -250 | set on | | 0,2,5 | | | |
| | | 200 | hi = add 200 V | 4 | 2 | | -200 | set on | | 0,2 | | | |
| | | 500 | hi = add 500 V | 4 | 1 | | -150 | set on | | 0,3 | | | |
| | | | | | | | -100 | set on | | 0,4 | | | |
| **Ch3 Bias** | **power supply 3c** | **control bits** | | | | | -50 | set on | | 0,5 | | | |
| Do not set OFF for 0 volts as this will turn off the bias on the other channels also. | | | | | | | 0 | set Lo bits 1 through 5 | | | | | |
| | | ± | Hi = negative | 5 | 0 | | 50 | set on | | 5 | | | |
| | | 50 | hi = add 50 V | 5 | 5 | | 100 | set on | | 4 | | | |
| | | 100 | hi = add 100 V | 5 | 4 | | 150 | set on | | 3 | | | |
| | | 150 | hi = add 150 V | 5 | 3 | | 200 | set on | | 2 | | | |
| | | 200 | hi = add 200 V | 5 | 2 | | 250 | set on | | 2,5 | | | |
| | | 500 | hi = add 500 V | 5 | 1 | | 300 | set on | | 2,4 | | | |
| | | | | | | | 350 | set on | | 2,3 | | | |
| | | | | | | | 400 | set on | | 2,3,5 | | | |
| **Ch4 Bias** | **power supply 3d** | **control bits** | | | | | 450 | set on | | 2,3,4 | | | |
| Do not set OFF for 0 volts as this will turn off the bias on the other channels also. | | | | | | | 500 | set on | | 1 | | | |
| | | ± | Hi = negative | 6 | 0 | | 550 | set on | | 1,5 | | | |
| | | 50 | hi = add 50 V | 6 | 5 | | 600 | set on | | 1,4 | | | |
| | | 100 | hi = add 100 V | 6 | 4 | | 650 | set on | | 1,3 | | | |
| | | 150 | hi = add 150 V | 6 | 3 | | 700 | set on | | 1,2 | | | |
| | | 200 | hi = add 200 V | 6 | 2 | | 750 | set on | | 1,2,5 | | | |
| | | 500 | hi = add 500 V | 6 | 1 | | 800 | set on | | 1,2,4 | | | |
| | | | | | | | 850 | set on | | 1,2,3 | | | |
| | | | | | | | 900 | set on | | 1,2,3,5 | | | |
| | | | | | | | 950 | set on | | 1,2,3,4 | | | |
| | | | | | | | 1000 | set on | | 1,2,3,4,5 | | | |
| | | | | | | | | | | | | | |

Figure 17 $I^2C$ addresses

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **PCD** | **power supply 4** | **control bits** | | | | | **voltage** | | | **set bits hi** | | | |
| | | | | | | | 0 | set off | | | | | |
| | | 100 | Hi = add 100 V | 3 | 7 | | 100 | set on | | A3,B7 | | | |
| | | 200 | Hi = add 200 V | 3 | 6 | | 200 | set on | | A3,B6 | | | |
| | | 300 | Hi = add 300 V | 0 | 7 | | 300 | set on | | A0,B7 | | | |
| | | 400 | Hi = add 400 V | 0 | 6 | | 400 | set on | | A0,B6 | | | |
| | | | | | | | 500 | set on | | A0,B6+A3,B7 | | | |
| | | | | | | | 600 | set on | | A0,B6+A3,B6 | | | |
| | | | | | | | 700 | set on | | A0,B6+A0,B7 | | | |
| | | | | | | | 800 | set on | | A0,B6+A0,B7+A3,B7 | | | |
| | | | | | | | 900 | set on | | A0,B6+A0,B7+A3,B6 | | | |
| | | | | | | | 1000 | set on | | A0,B6+A0,B7+A3,B6+A3,B7 | | | |
| **Analogue read of power rails** | | | | Address | input | inputs go from 0 through 3 | | | | | | | |
| **phosphor** | power supply 1 | | | 0 | 1 | | volts = reading*11.76 | | | | | | |
| **Spare** | Power supply 2 | | No monitor | | | | | | | | | | |
| **Ch1 Bias** | power supply 3a | | | 1 | 0 | | **volts= (reading -127)*8.1** | | | | | | |
| **Ch2 Bias** | power supply 3b | | | 1 | 1 | | **volts= (reading -127)*8.1** | | | | allow for several | | |
| **Ch3 Bias** | power supply 3c | | | 1 | 2 | | **volts= (reading -127)*8.1** | | | | different values of the gain | | |
| **Ch4 Bias** | power supply 3d | | | 1 | 3 | | **volts= (reading -127)*8.1** | | | | | | |
| **PCD** | power supply 4 | | | 0 | 3 | | volts = (reading -255)*3.92 | | | | e.g. one for each polarity | | |
| **pulser -4kV** | power supply 5 | | | 0 | 2 | | volts = reading*15.69 | | | | and one for each channel | | |
| **pulser -3kV** | power supply 6 | | | 0 | 0 | | volts = (reading -255)*11.76 | | | | | | |
| **use** | | **operation** | **sense** | **address** | **bit** | | | | | | | | |
| trigger Inhibit | | inhibit/enable | Lo = inhibit | 7 | 0 | | | | | | | | |

Figure 18 $I^2C$ addresses

| use | | operation | delay ps | sense | | address | bit | | | Delay | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **delay Unit** | **USES 8574A** | | | | | | | | | | | | |
| channel 1 | | insert delay | 50 | Lo = insert | | A3 | 0 | | | | | | |
| | | | 100 | Lo = insert | | A3 | 1 | | | | | | |
| | | | 200 | Lo = insert | | A3 | 2 | send byte = | | 255-(delay/50ps) | | | |
| | | | 400 | Lo = insert | | A3 | 3 | | | | | | |
| | | | 800 | Lo = insert | | A3 | 4 | | | | | | |
| | | | 1600 | Lo = insert | | A3 | 5 | | | | | | |
| | | | 3200 | Lo = insert | | A3 | 6 | | | | | | |
| channel 2 | | insert delay | 50 | Lo = insert | | A2 | 0 | | | | | | |
| | | | 100 | Lo = insert | | A2 | 1 | | | | | | |
| | | | 200 | Lo = insert | | A2 | 2 | send byte = | | 255-(delay/50ps) | | | |
| | | | 400 | Lo = insert | | A2 | 3 | | | | | | |
| | | | 800 | Lo = insert | | A2 | 4 | | | | | | |
| | | | 1600 | Lo = insert | | A2 | 5 | | | | | | |
| | | | 3200 | Lo = insert | | A2 | 6 | | | | | | |
| channel 3 | | insert delay | 50 | Lo = insert | | A1 | 0 | | | | | | |
| | | | 100 | Lo = insert | | A1 | 1 | | | | | | |
| | | | 200 | Lo = insert | | A1 | 2 | send byte = | | 255-(delay/50ps) | | | |
| | | | 400 | Lo = insert | | A1 | 3 | | | | | | |
| | | | 800 | Lo = insert | | A1 | 4 | | | | | | |
| | | | 1600 | Lo = insert | | A1 | 5 | | | | | | |
| | | | 3200 | Lo = insert | | A1 | 6 | | | | | | |
| channel 4 | | insert delay | 50 | Lo = insert | | A0 | 0 | | | | | | |
| | | | 100 | Lo = insert | | A0 | 1 | | | | | | |
| | | | 200 | Lo = insert | | A0 | 2 | send byte = | | 255-(delay/50ps) | | | |
| | | | 400 | Lo = insert | | A0 | 3 | | | | | | |
| | | | 800 | Lo = insert | | A0 | 4 | | | | | | |
| | | | 1600 | Lo = insert | | A0 | 5 | | | | | | |
| | | | 3200 | Lo = insert | | A0 | 6 | | | | | | |
| | | | **Low voltage Power supply checks** | | | | | | | | | | |
| **Check that 12 volts is getting to Auxillary psu box** | | | | **address** | **bit** | | result | | | | | | |
| | | | Turn Off PSUs 3a,b,c,d Then | | | | | | | | | | |
| | | | Write Hi to | 5 | 7 | | | | | | | | |
| | | | **READ** | 5 | 7 | | Hi= ON | | | | | | |
| | | | | | | | Lo = OFF | | | | | | |
| | **note that the clock from PSU3a can make this level Hi even when it is not on.** | | | | | | | | | | | | |
| **Check that Clock from main PSU is connected to AUX psu** | | | Write Hi to | 5 | 8 | | | | | | | | |
| | | | READ | 5 | 8 | | Hi = ON | | | | | | |
| | | | | | | | Lo= OFF | | | | | | |
| **Check 15 volt rail regulator for power supplies and delay unit** | | | | | | | | | | | | | |
| | | This is not on the I2C bus | | address 0 input 0 | | | | | | | | | |
| | | use command A-D | | Voltage OK gives | | 765 | to | 840 | | | | | |
| | | | | Voltage OFF gives | | 95 | to | 99 | | | | | |
| Note: | | | | | | | | | | | | | |
| If the pulser is run at a significant rep. Rate then the power supply takes more current and the external supply may have to be increased to maintain the 765 count. | | | | | | | | | | | | | |

Figure 19 I$^2$C addresses

## APPENDIX 1 ADJUSTMENT OF THE POWER SUPPLY MAXIMUM VOLTAGES

**The detector head should be removed for all the work in this appendix. Failure to do so could damage the head.**

The maximum voltage that each power supply can be set to is adjustable. The controls are however, not very accessible. Also in the case or power rails 3a and 4 it is not possible to have computer control of the supply during adjustment.

When adjusting the maximum voltages it is important that the loads be disconnected as it is possible to exceed significantly the rated voltage of the loads used.

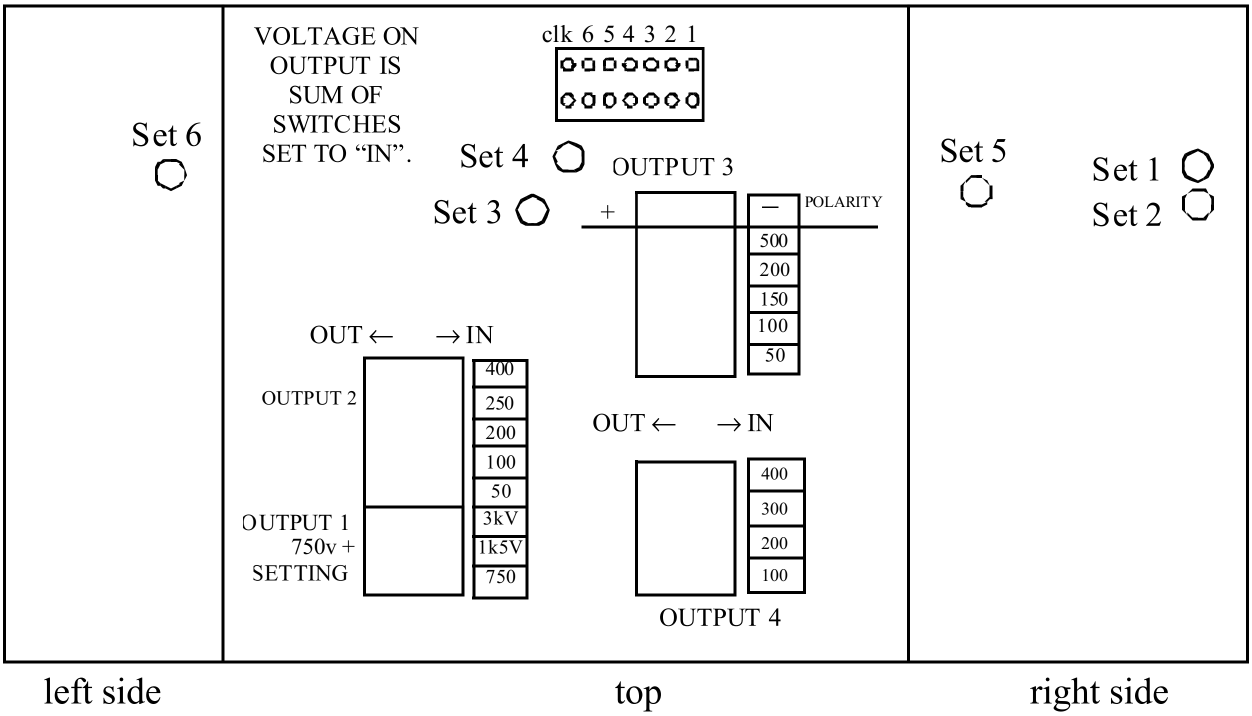



Figure 20 Power supply controls

To adjust supplies 1,2,5 and 6 access to the adjustment potentiometers is available along the sides of the main power supply. One or more of the straps that hold the interface board down may need to be removed temporarily.

**Supplies 5 and 6 are used for the pulse generator and should not normally be adjusted unless we have recommended this to be done.**

When adjusting supplies it is best to set the voltage to the maximum with the software. In order to adjust rails 4 and 3a the interface board must be removed. It is then necessary to enable these two supplies manually by connecting together the relevant two pins in the "on/off control" socket, see figure 20. The voltage will automatically be at its maximum setting (as the software would do it) as the manual controls for these rails are high when disconnected.

Note that if the computer is still running and monitoring the voltages it is possible to have the monitors indicating the voltages on the rail being adjusted even when the control interface board is removed.

Adjustment of rails 3b,c,d is also possible but there is no access to the controls without removing the electrical protection of the box (the Auxiliary power supply box). This procedure is therefore open to risk of electrical shock and should not be attempted unless the user is familiar with operating on live high voltage supplies. The voltage can only reach around 1100 volts and the current is small.

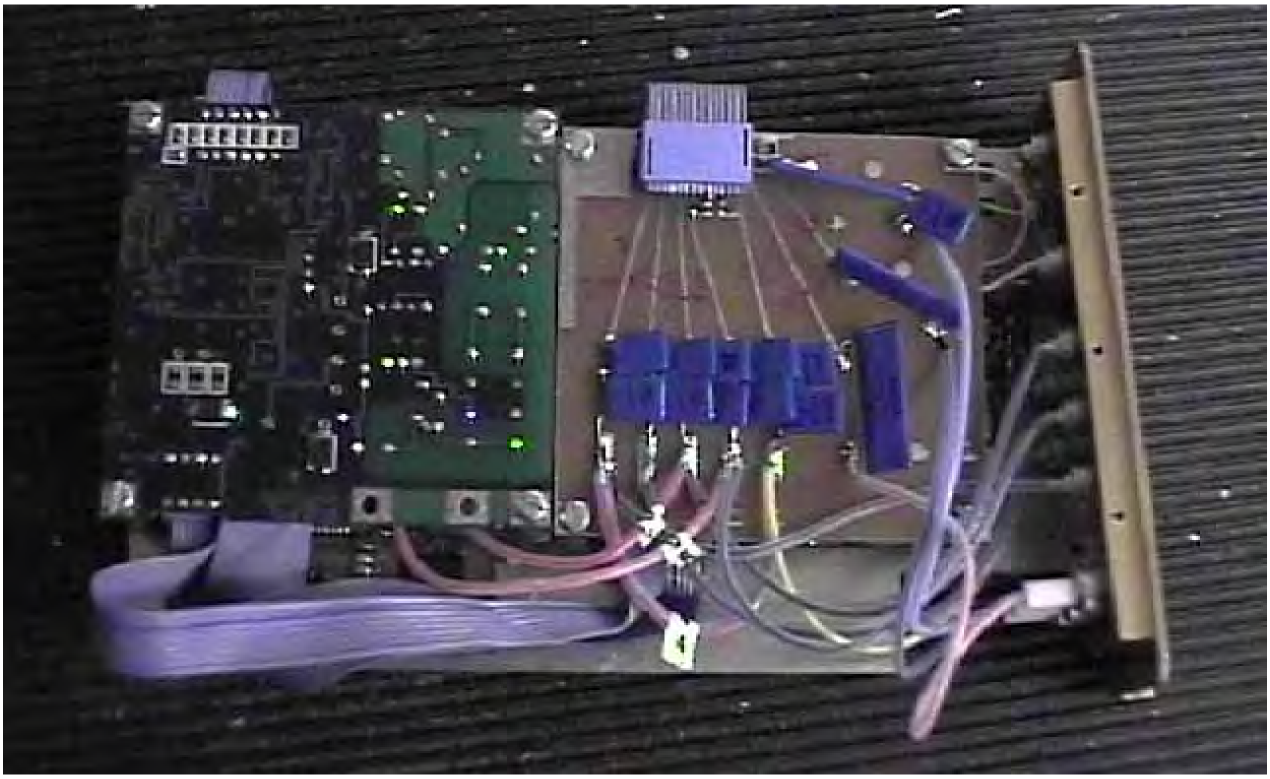


Figure 21 The inside of the Auxiliary power supply.

Figure 22 Maximum voltage adjustment potentiometers.
The third is accessible from the other side.

**Before removing the cover of the Auxiliary power supply it is essential that all the connections from the main supply are removed, particularly the power rails 1, 5 and 6. These are higher voltage rails and two have significant current capability. They will hurt a lot if touched.**

The following is a sequence of operations to adjust these three rails:-

1) With the cart running normally execute a “SAFE” command and check that all voltages are zero with a “?STATUS” command.

2) Remove the screws holding the box to the cart.

3) Remove all connectors from the front panel and disconnect the head as this procedure will require the maximum voltages to be applied to the bias outputs.

4) Remove the outer cover (three or four screws around the edge of the front panel hold it in).

5) place the unit on an insulating surface. Be careful about stressing the connections to the front panel, particularly those to the PCB mounted 4 way connector for the $I^2C$ bus.

6) Reconnect the $I^2C$ bus lead, the 12 volt lead and the clock/inhibit lead.

7) Locate the three potentiometers that need adjustment. See figure 22.

8) Connect a high voltage probe to the output to be adjusted.

9) Execute a command string as follows:-

1000 1000 1000 1000 !HVBIAS1234

This will place all four bias supplies at the maximum positive voltage. Note that one cannot have just one supply at a time at 1000 volts unless the bias limit is set to 1000 volts. This is dangerous as one may forget to return it to the normal value. However, running all four bias supplies at 1000 volts also means that more points in the supply are at a high voltage. Exercise extreme care.

10) Adjust the voltage as required with a well insulated trimming tool..

11) Repeat the procedure with the supplies at -1000 volts. There is only one control for both polarities. An optimum setting must be found.

12) Execute a “SAFE” command before disconnecting the Auxiliary power supply again and e-assembling.

13) When re-assembling make sure to include the plastic cover over the top of the Auxiliary power supply boards. The monitor board has up to 6kV applied to it and may break down to the case without this plastic cover.

14) When sliding the boards back into the cover make sure not to damage the ribbon cable links particularly the small link shown at the top left in figure 21.

## APPENDIX 2 FITTING A REPLACEMENT EPROM

Should it become necessary to change the EPROM the following instructions should be adhered to. Changing the EPROM is only likely to be necessary if the software needs to be changed significantly. Small changes to the software are easily down loaded every time the system is booted up.

The following is a simple list of operations:-

1 Locate the computer box. If the cart has not been modified it is the lower front box as shown below.

2 Turn off all the power (both 15 volt rails)

3 Remove the three screws on the end panel (opposite end to the connector panel).

4 Remove the four screws holding the box to the cart.

5 Remove the three screws holding the connector panel in the box (the aluminium extrusion)

6 Slide the aluminium extrusion back to reveal the EPROM. The EPROM is shown in figure 23e.

Note that it is not necessary to remove all the connectors from the connector panel.

7 Carefully lever out the old EPROM and put to one side in an antistatic container. Put the new EPROM into the socket maintaining the correct orientation, see figure 23e. If necessary use a suitable IC insertion tool.

8 Replace the cover making sure the board is in the bottom slot as shown in figure 23g.

9 Replace the screws in the end panel, see figure 23f. This may require some juggling or even removal of the board to straighten the regulator leads. Do not tighten.

10 Replace the screws in the outer cover and then tighten the screws into the regulators.

11 Replace the screws holding the box to the cart.

12 Power up just the μ Processor power and check that the Processor is behaving suitably before proceeding to turn on the main power to the rest of the cart.

13 Store the old EPROM for safe keeping in case the new one has errors in it.

Figure 23 Replacing the EPROM

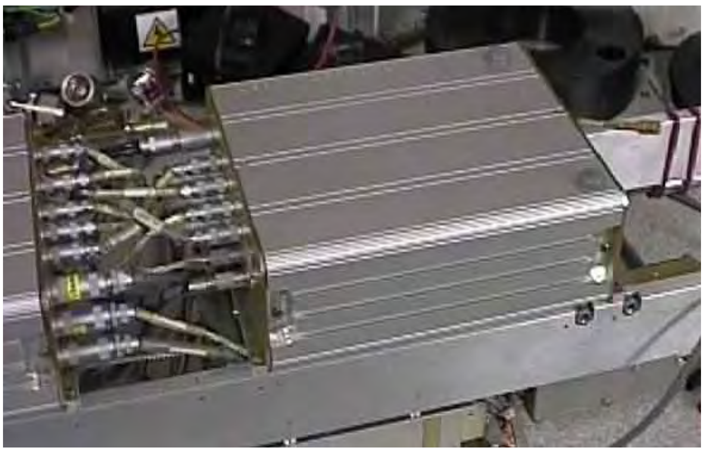


Figure 23a
Locate the computer box

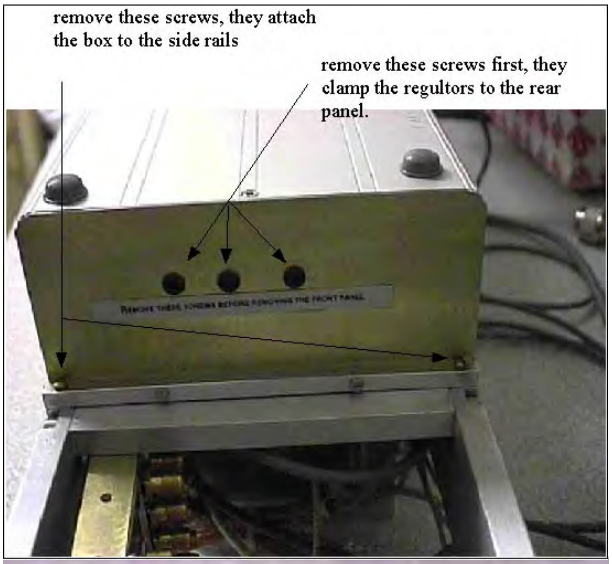



Figure 23b
Remove the regulator clamp screws and the box fixing screws

Figure 23c
Remove the three screws holding the connector panel.

Figure 23d
Slide the box away. It is not necessary to remove the connectors from the panel.


Figure 23e
Locate the EPROM and replace.
Note the orientation of the chip

Figure 23f
Make sure the regulators are not bent down before re-assembly

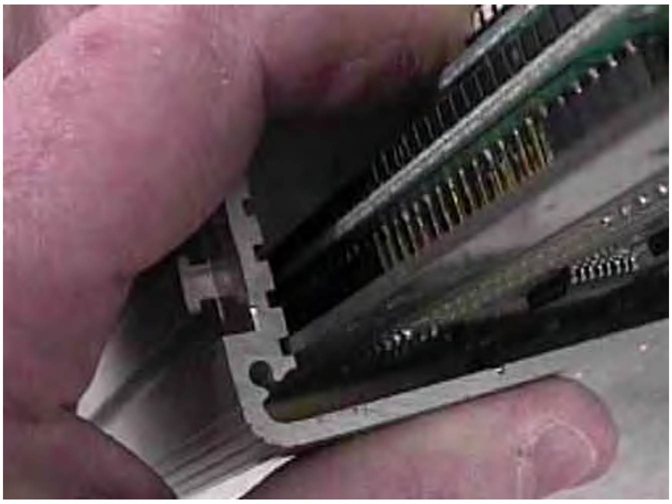
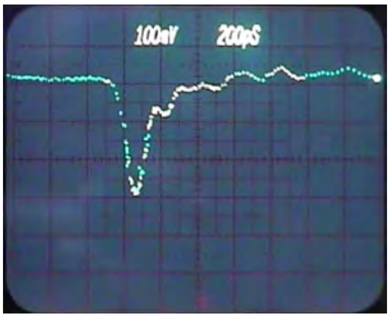


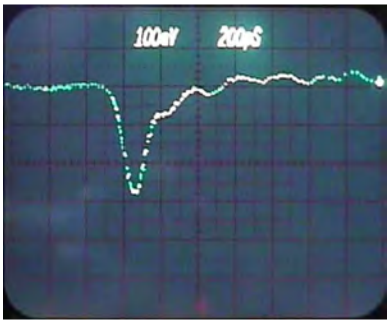
Figure 23g
Make sure the board slides back into the correct slot on re-assembly. Also make sure the box is up the correct way.

**APPENDIX 3 OUTPUT PULSE SHAPES**

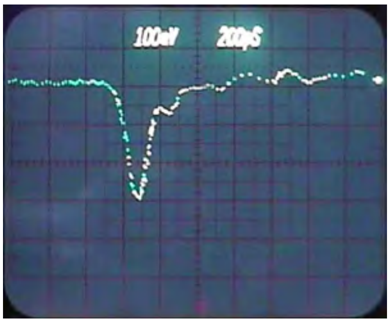
Figure 24 Unit 1 100ps modules



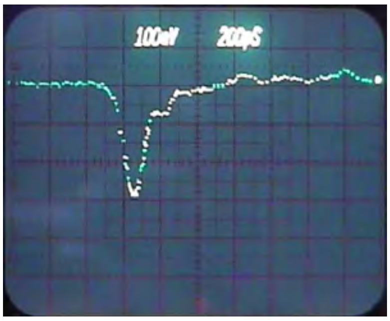

ch1




ch2

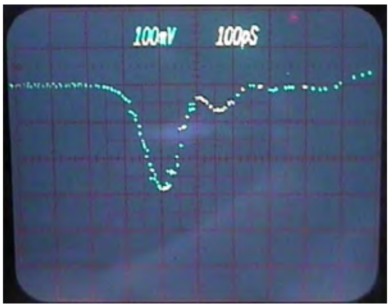



ch3

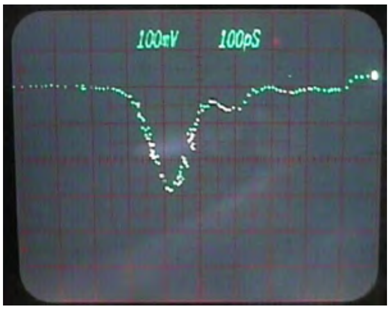



ch 4

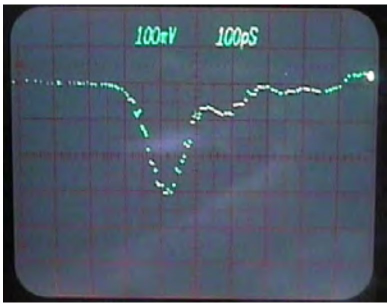
Figure 25 Unit 2 100ps modules



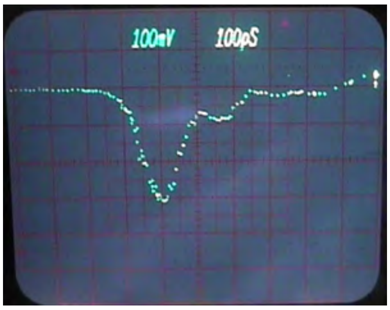

ch1




ch2

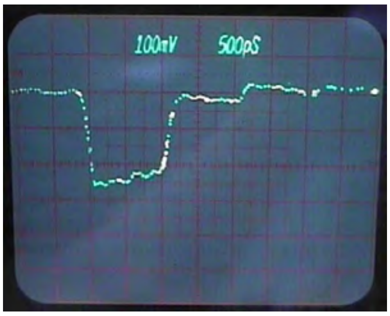



ch3

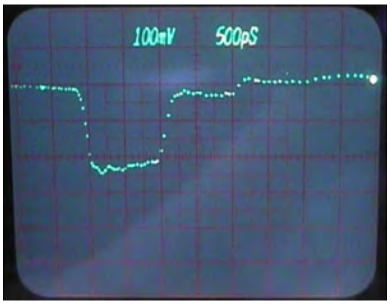



ch 4

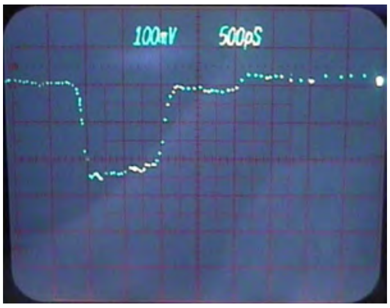
Figure 26 Unit 2 1ns modules



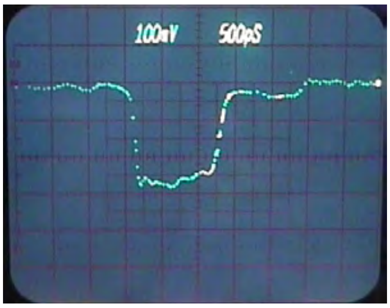

ch1




ch2




ch3




ch 4

Basic cable lengths in delay unit, units of ps J9912231/1

| ch1 | ch2 | ch3 | ch4 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 90 | 10 | 10 | 10 |
| 160 | 40 | 20 | 50 |
| 380 | 10 | 0 | 20 |
| 760 | -10 | -10 | 0 |
| 1500 | 60 | 0 | 20 |
| 3075 | 100 | 10 | 10 |
| 6100 | 110 | -50 | -40 |

| | | differences | | |
|---|---|---|---|---|
| delay setting | ch1 | ch2 | ch3 | ch4 |
| 0 | 0 | 0 | 0 | 0 |
| 100 | 90 | 10 | 10 | 10 |
| 200 | 160 | 40 | 20 | 50 |
| 300 | 250 | 50 | 30 | 60 |
| 400 | 380 | 10 | 0 | 20 |
| 500 | 470 | 20 | 10 | 30 |
| 600 | 540 | 50 | 20 | 70 |
| 700 | 630 | 60 | 30 | 80 |
| 800 | 760 | -10 | -10 | 0 |
| 900 | 850 | 0 | 0 | 10 |
| 1000 | 920 | 30 | 10 | 50 |
| 1100 | 1010 | 40 | 20 | 60 |
| 1200 | 1140 | 0 | -10 | 20 |
| 1300 | 1230 | 10 | 0 | 30 |
| 1400 | 1300 | 40 | 10 | 70 |
| 1500 | 1390 | 50 | 20 | 80 |
| 1600 | 1500 | 60 | 0 | 20 |
| 1700 | 1590 | 70 | 10 | 30 |
| 1800 | 1660 | 100 | 20 | 70 |
| 1900 | 1750 | 110 | 30 | 80 |
| 2000 | 1880 | 70 | 0 | 40 |
| 2100 | 1970 | 80 | 10 | 50 |
| 2200 | 2040 | 110 | 20 | 90 |
| 2300 | 2130 | 120 | 30 | 100 |
| 2400 | 2260 | 50 | -10 | 20 |
| 2500 | 2350 | 60 | 0 | 30 |
| 2600 | 2420 | 90 | 10 | 70 |
| 2700 | 2510 | 100 | 20 | 80 |
| 2800 | 2640 | 60 | -10 | 40 |
| 2900 | 2730 | 70 | 0 | 50 |
| 3000 | 2800 | 100 | 10 | 90 |
| 3100 | 2890 | 110 | 20 | 100 |
| 3200 | 3075 | 100 | 10 | 10 |
| 3300 | 3165 | 110 | 20 | 20 |
| 3400 | 3235 | 140 | 30 | 60 |
| 3500 | 3325 | 150 | 40 | 70 |
| 3600 | 3455 | 110 | 10 | 30 |
| 3700 | 3545 | 120 | 20 | 40 |
| 3800 | 3615 | 150 | 30 | 80 |
| 3900 | 3705 | 160 | 40 | 90 |
| 4000 | 3835 | 90 | 0 | 10 |
| 4100 | 3925 | 100 | 10 | 20 |
| 4200 | 3995 | 130 | 20 | 60 |
| 4300 | 4085 | 140 | 30 | 70 |
| 4400 | 4215 | 100 | 0 | 30 |
| 4500 | 4305 | 110 | 10 | 40 |
| 4600 | 4375 | 140 | 20 | 80 |
| 4700 | 4465 | 150 | 30 | 90 |
| 4800 | 4575 | 160 | 10 | 30 |
| 4900 | 4665 | 170 | 20 | 40 |
| 5000 | 4735 | 200 | 30 | 80 |
| 5100 | 4825 | 210 | 40 | 90 |
| 5200 | 4955 | 170 | 10 | 50 |
| 5300 | 5045 | 180 | 20 | 60 |
| 5400 | 5115 | 210 | 30 | 100 |
| 5500 | 5205 | 220 | 40 | 110 |
| 5600 | 5335 | 150 | 0 | 30 |
| 5700 | 5425 | 160 | 10 | 40 |
| 5800 | 5495 | 190 | 20 | 80 |
| 5900 | 5585 | 200 | 30 | 90 |
| 6000 | 5715 | 160 | 0 | 50 |
| 6100 | 5805 | 170 | 10 | 60 |
| 6200 | 5875 | 200 | 20 | 100 |
| 6300 | 5965 | 210 | 30 | 110 |

| | | differences | | |
|---|---|---|---|---|
| delay setting | ch1 | ch2 | ch3 | ch4 |
| 6400 | 6100 | 110 | -50 | -40 |
| 6500 | 6190 | 120 | -40 | -30 |
| 6600 | 6260 | 150 | -30 | 10 |
| 6700 | 6350 | 160 | -20 | 20 |
| 6800 | 6480 | 120 | -50 | -20 |
| 6900 | 6570 | 130 | -40 | -10 |
| 7000 | 6640 | 160 | -30 | 30 |
| 7100 | 6730 | 170 | -20 | 40 |
| 7200 | 6860 | 100 | -60 | -40 |
| 7300 | 6950 | 110 | -50 | -30 |
| 7400 | 7020 | 140 | -40 | 10 |
| 7500 | 7110 | 150 | -30 | 20 |
| 7600 | 7240 | 110 | -60 | -20 |
| 7700 | 7330 | 120 | -50 | -10 |
| 7800 | 7400 | 150 | -40 | 30 |
| 7900 | 7490 | 160 | -30 | 40 |
| 8000 | 7600 | 170 | -50 | -20 |
| 8100 | 7690 | 180 | -40 | -10 |
| 8200 | 7760 | 210 | -30 | 30 |
| 8300 | 7850 | 220 | -20 | 40 |
| 8400 | 7980 | 180 | -50 | 0 |
| 8500 | 8070 | 190 | -40 | 10 |
| 8600 | 8140 | 220 | -30 | 50 |
| 8700 | 8230 | 230 | -20 | 60 |
| 8800 | 8360 | 160 | -60 | -20 |
| 8900 | 8450 | 170 | -50 | -10 |
| 9000 | 8520 | 200 | -40 | 30 |
| 9100 | 8610 | 210 | -30 | 40 |
| 9200 | 8740 | 170 | -60 | 0 |
| 9300 | 8830 | 180 | -50 | 10 |
| 9400 | 8900 | 210 | -40 | 50 |
| 9500 | 8990 | 220 | -30 | 60 |
| 9600 | 9175 | 210 | -40 | -30 |
| 9700 | 9265 | 220 | -30 | -20 |
| 9800 | 9335 | 250 | -20 | 20 |
| 9900 | 9425 | 260 | -10 | 30 |
| 10000 | 9555 | 220 | -40 | -10 |
| 10100 | 9645 | 230 | -30 | 0 |
| 10200 | 9715 | 260 | -20 | 40 |
| 10300 | 9805 | 270 | -10 | 50 |
| 10400 | 9935 | 200 | -50 | -30 |
| 10500 | 10025 | 210 | -40 | -20 |
| 10600 | 10095 | 240 | -30 | 20 |
| 10700 | 10185 | 250 | -20 | 30 |
| 10800 | 10315 | 210 | -50 | -10 |
| 10900 | 10405 | 220 | -40 | 0 |
| 11000 | 10475 | 250 | -30 | 40 |
| 11100 | 10565 | 260 | -20 | 50 |
| 11200 | 10675 | 270 | -40 | -10 |
| 11300 | 10765 | 280 | -30 | 0 |
| 11400 | 10835 | 310 | -20 | 40 |
| 11500 | 10925 | 320 | -10 | 50 |
| 11600 | 11055 | 280 | -40 | 10 |
| 11700 | 11145 | 290 | -30 | 20 |
| 11800 | 11215 | 320 | -20 | 60 |
| 11900 | 11305 | 330 | -10 | 70 |
| 12000 | 11435 | 260 | -50 | -10 |
| 12100 | 11525 | 270 | -40 | 0 |
| 12200 | 11595 | 300 | -30 | 40 |
| 12300 | 11685 | 310 | -20 | 50 |
| 12400 | 11815 | 270 | -50 | 10 |
| 12500 | 11905 | 280 | -40 | 20 |
| 12600 | 11975 | 310 | -30 | 60 |
| 12700 | 12065 | 320 | -20 | 70 |

Figure 27 Measured delays versus set delays.
Only the 8 delays created by individual delay cables were measured.
The rest are calculated from these results.

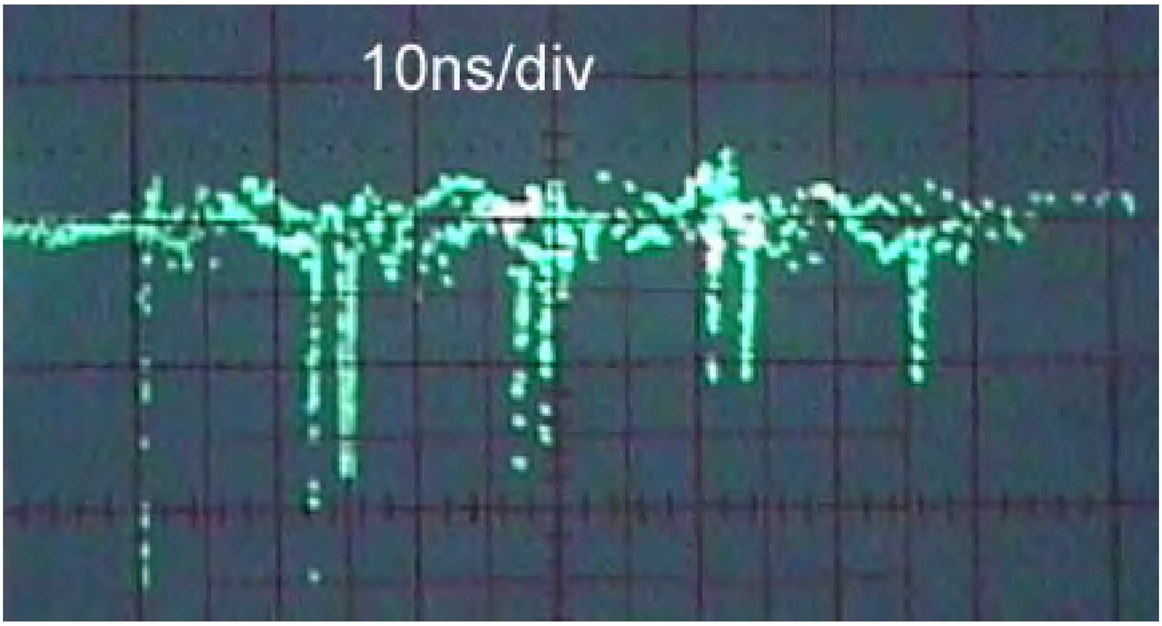
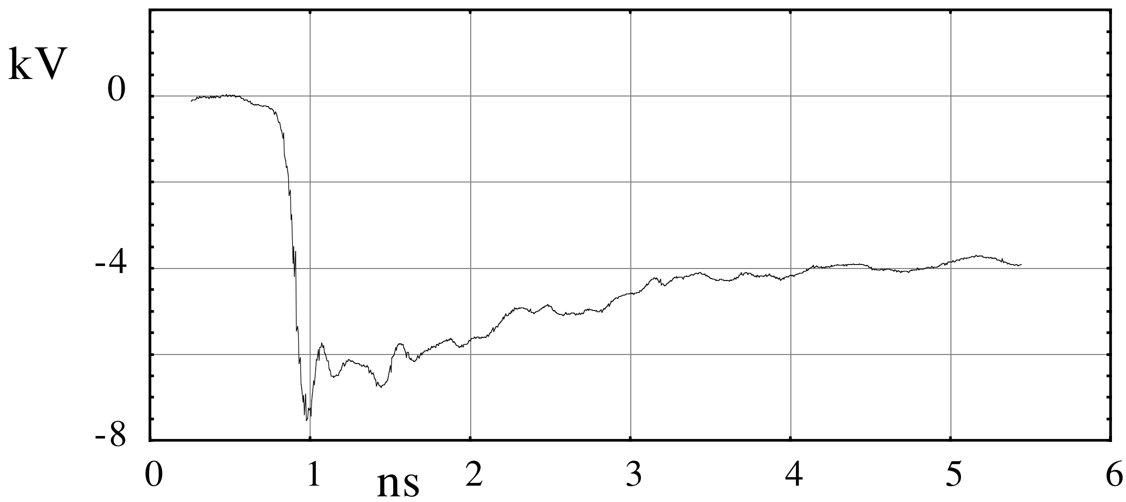



Figure 28 Monitor outputs with just the four pulse channels driven.
This superposition of two sets of data, taken at minimum and maximum delay settings, shows the four 15ns windows created by the delay cables.
Pulses are, from left to right:-

1 channel 1 zero delay
2 channel 1 12.7ns delay set
3 channel 2 zero delay
4 channel 2 12.7ns delay set
5 channel 3 zero delay
2 channel 3 12.7ns delay set
1 channel 4 zero delay
8 channel 5 12.7ns delay set

# Typical unformed pulse




# Typical unformed pulse

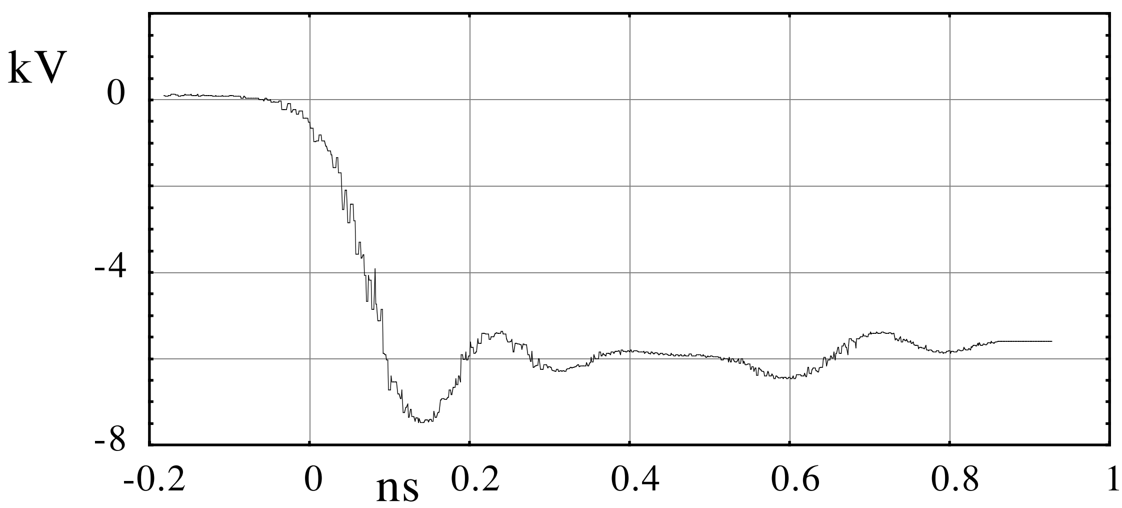



Figure 29 Unformed output pulses

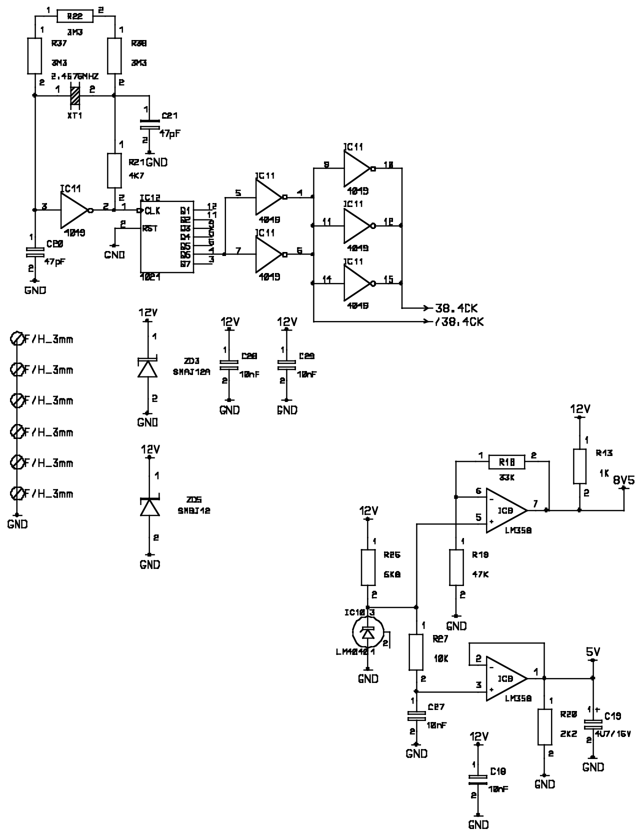
This unit has three build variants:-
Master
Half master
Slave

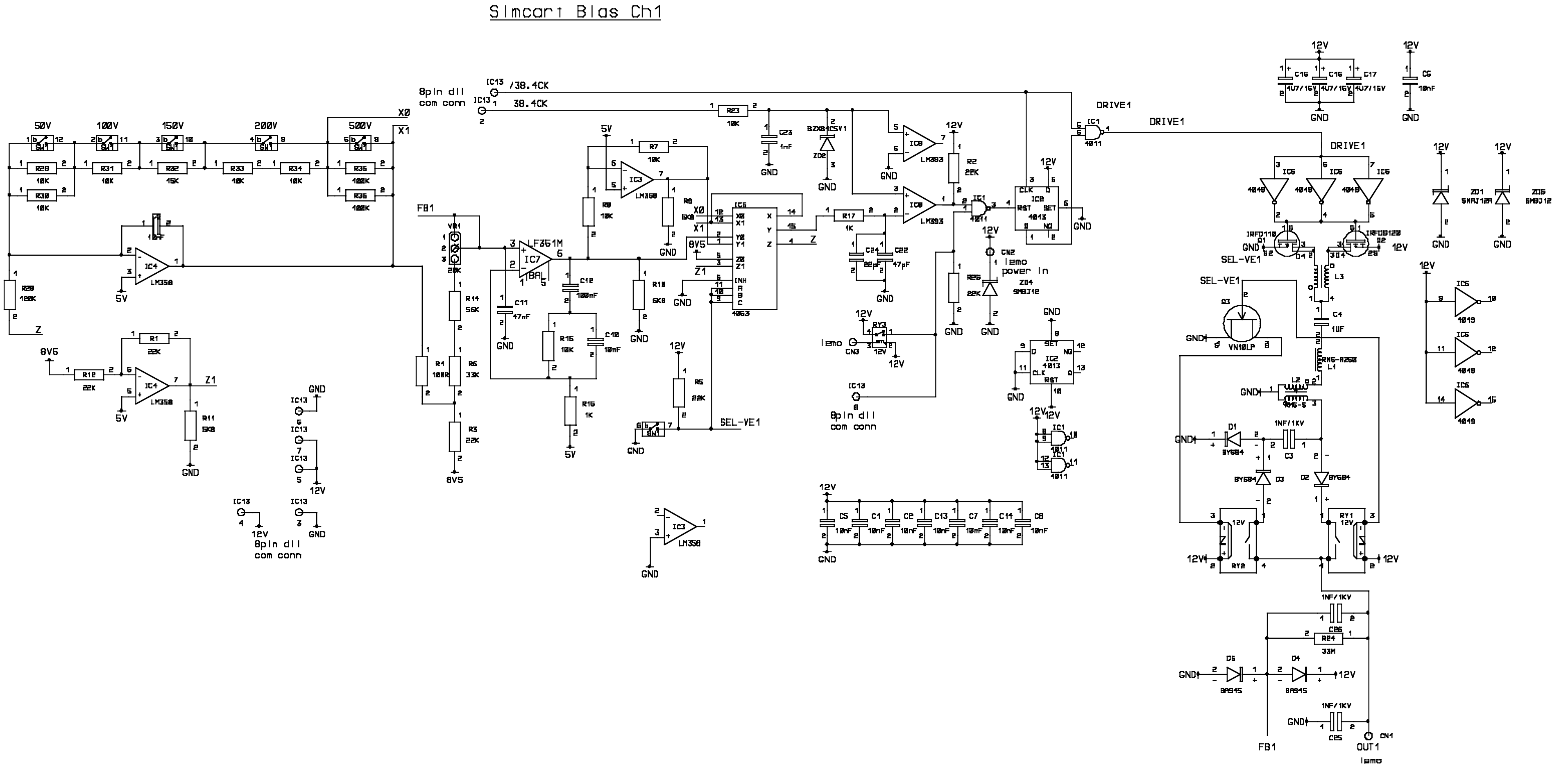
**Master** contains all the elements above.
**Half master** does not contain the clock circuit. The clock is brought in from outside into pins 4 and 6 of IC 11; pins 5 and 7 are dicsonnected from IC12 and grounded.
**Slave** does not contain IC11 either and clock and clock bar are both brought in from outside.

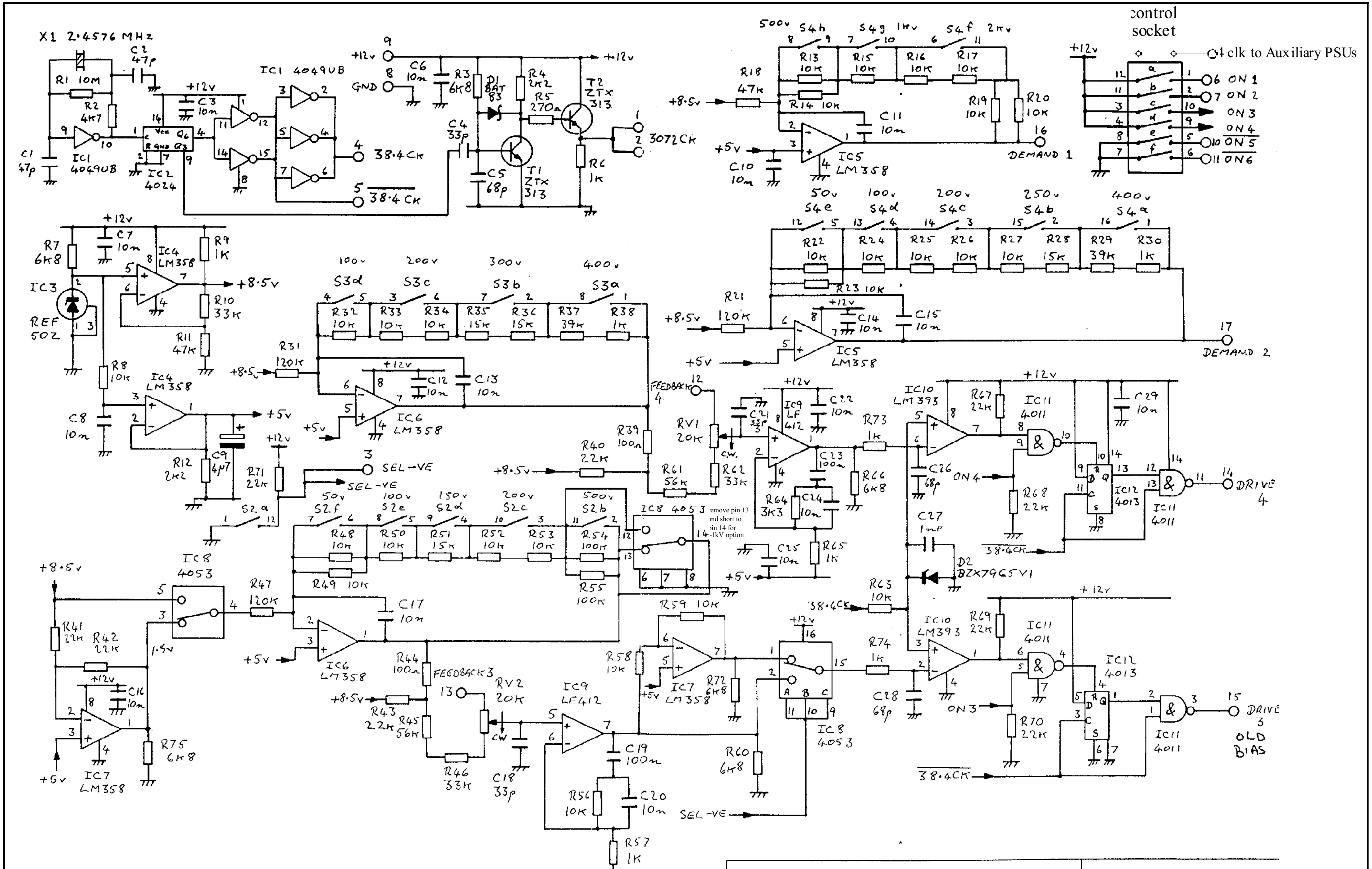
**Uses.**
As a stand alone PSU the Master is used.
As a multichannel system there is one master that is linked via an 8 pin DIP to the slaves.

On Simcart upgrades which retain one bias supply in the main power supply the extra three bias rails are supplied by one half master and two slaves. The Clock output from the existing main power supply is fed into the half master as described above. The incomming clock is treated as clock bar by these extra units. The new clock buffered by IC 11 on the half master is then distributed to the slaves along with the incoming clock bar signal.

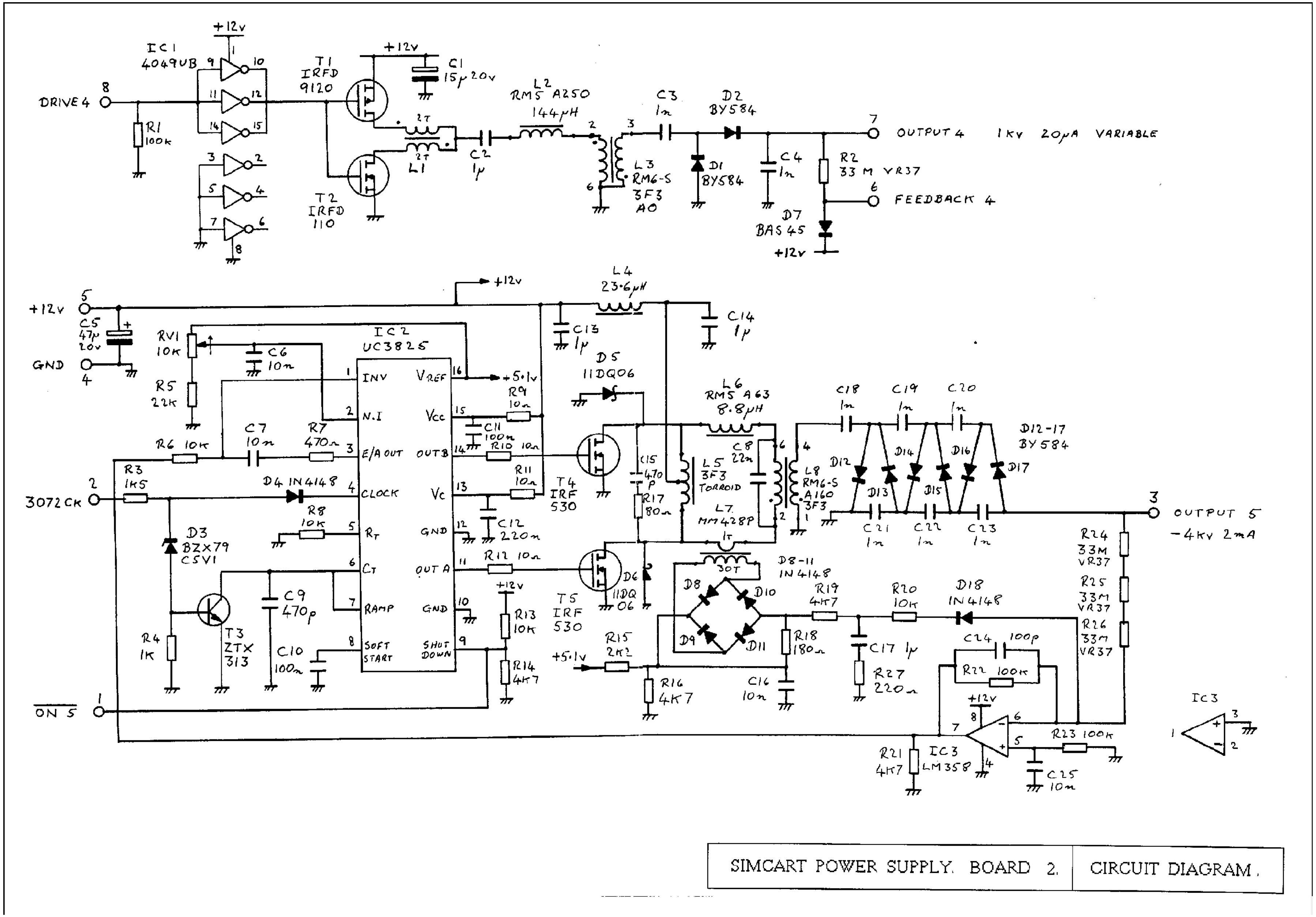
In this manner the extra three bias rails are synchronous with the main power supply so stopping rails talking to each other and also the bias inhibit to the main power supply is used to enable/disable the extra three units by turning the clock output from the main supply off . With the clock off, the clock line goes high and this can be read by the computer to establish if the clock line is connected to the main power supply.

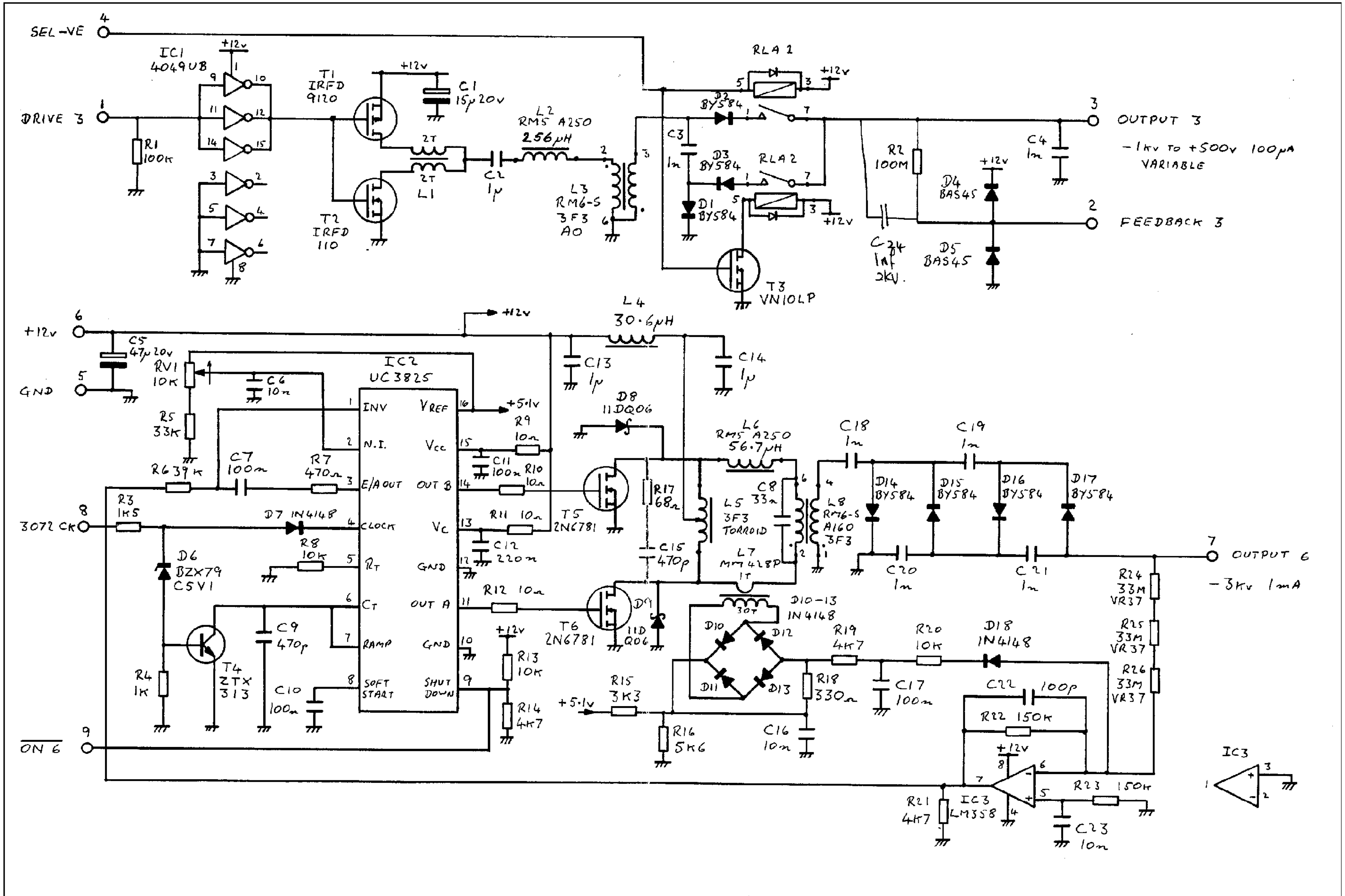



Simcart Bias Ch1
8pin dil
com conn
/38.4CK
38.4CK
DRIVE1
SEL-VE1
FB1
OUT1
lemo
power in
50V
100V
150V
200V
500V
LF351M
LM358
LM393
4053
4013
4011
4049
IRFD110
IRFD9120
VN10LP
BYG04
BAS45
1NF/1KV
12V
GND
5V
8V5

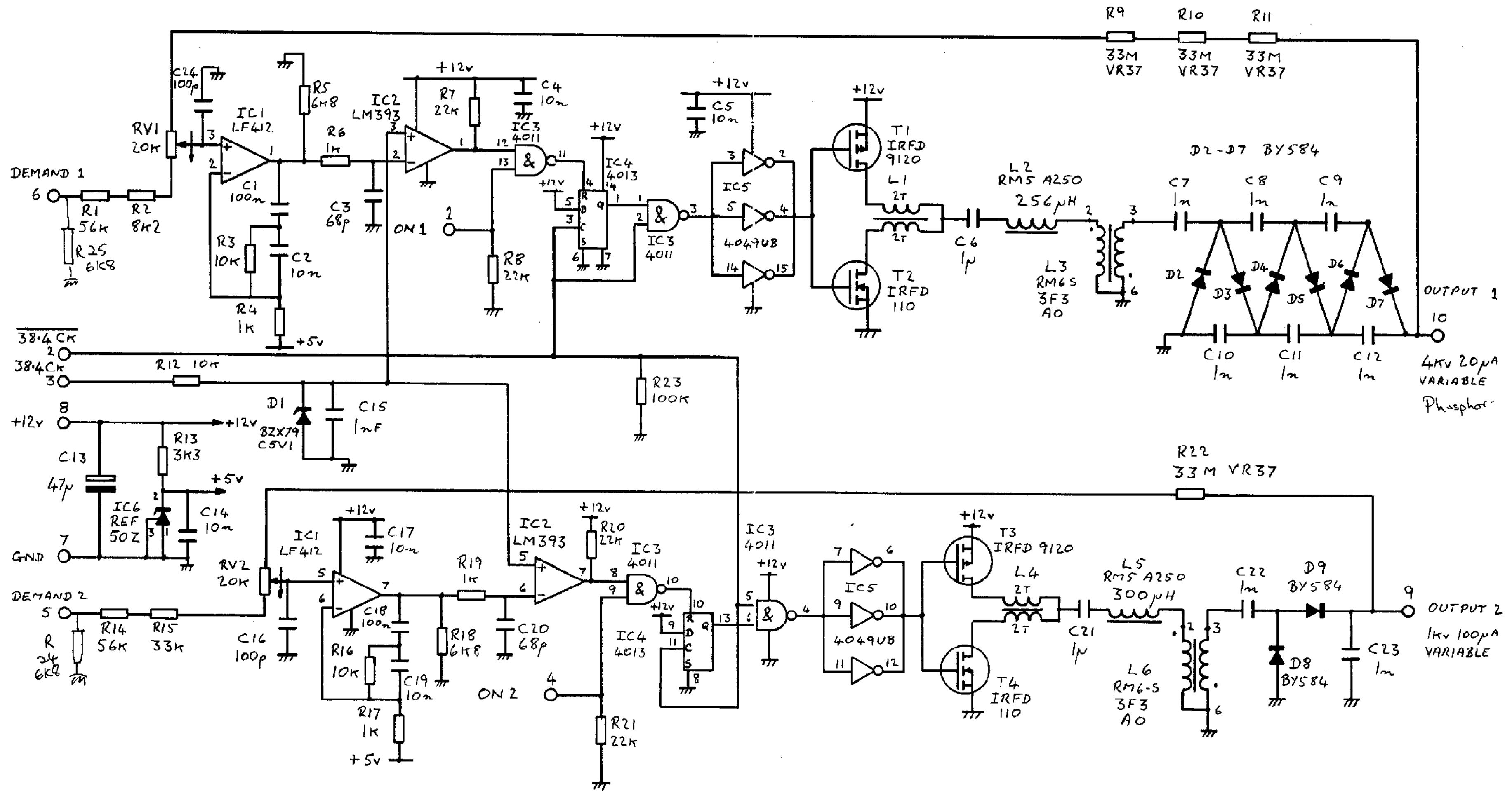



SIMCART POWER SUPPLY. BOARD 1. | CIRCUIT DIAGRAM.


SIMCART POWER SUPPLY. BOARD 2.
CIRCUIT DIAGRAM.
IC1 4049UB
T1 IRFD 9120
T2 IRFD 110
C1 15µ 20v
L2 RMS A250 144µH
C3 1n
D2 BY584
L3 RM6-S 3F3 A0
D1 BY584
C4 1n
R2 33 M VR37
D7 BAS 45
OUTPUT 4 1kv 20µA VARIABLE
FEEDBACK 4
DRIVE 4
R1 100k
+12v
GND
C5 47µ 20v
RV1 10k
R5 22k
IC2 UC3825
C6 10n
L4 23·6µH
C13 1µ
C14 1µ
D5 11DQ06
L6 RMS A63 8.8µH
C18 1n
C19 1n
C20 1n
D12-17 BY584
C15 470p
R17 80Ω
L5 3F3 TORROID
L7 MM428P
L8 RM6-S A160 3F3
C21 1n
C22 1n
C23 1n
OUTPUT 5 -4kv 2mA
R24 33M VR37
R25 33M VR37
R26 33M VR37
R3 1k5
3072 CK
D4 1N4148
R6 10k
C7 10n
R7 470Ω
R8 10k
D3 BZX79 C5V1
T3 ZTX 313
R4 1k
C9 470p
C10 100n
R9 10Ω
C11 100n
R10 10Ω
R11 10Ω
C12 220n
R12 10Ω
T4 IRF 530
T5 IRF 530
D6 11DQ06
R13 10k
R14 4k7
D8-11 1N4148
R19 4k7
R20 10k
D18 1N4148
R18 180Ω
C17 1µ
R27 220Ω
R15 2k2
R16 4k7
C16 10n
+5·1v
C24 100p
R22 100k
R23 100k
IC3 LM358
R21 4k7
C25 10n
ON 5




SIMCART POWER SUPPLY. BOARD 3. | CIRCUIT DIAGRAM.




SIMCART POWER SUPPLY. BOARD 4. | CIRCUIT DIAGRAM.